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Conditional Boosting-Based, Low-Power Flip-Flop Design for Near-Threshold Voltage Management

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Abstract: *When the supply voltage is reduced to near the threshold, a conditional-boosting flip-flop is recommended for an ultralow voltage application. The proposed flip-flop employs voltage boosting to provide low delay and reduced performance variation in the near-threshold voltage region. By eliminating superfluous boosting processes, it further utilises conditional capture to lower switching power consumption. Results from experiments conducted in a 25-nm CMOS process showed that the proposed flip-flop could reduce latency by up to 72 percent, reduce performance variability by 75 percent due to process variation, and improve the energy-delay product by up to 67 percent at 25% switching activity, compared to traditional precharged differential flip-flops.*

Keywords: Near-threshold, flip-flops, and bootstrapping

I. INTRODUCTION

Keywords: For portable gadgets to last a long time on a limited power budget, energy-efficient computing is a must. Voltage scaling is an effective way to lower the power consumption of complementary metal-oxide semiconductor (CMOS) digital circuits [1]. Unfortunately, extensive voltage scaling, as in subthreshold computing, leads to significant performance degradation.

One practical approach to reducing power usage while considering latency is near-threshold computing [2]. Still, circuits working in the near-threshold voltage area may have undesired performance unpredictability and increased delay in many low-power, high-speed applications. Operating clocked timing elements, like as latches and flip-flops, in the near-IR range has a significant effect on performance metrics including setup time, hold time, and latency. These components are crucial in high-speed synchronous systems.

zone of criticality. The system's overall performance will be negatively affected by this. Capacitive boosting has the potential to fix the problems caused by aggressive voltage scaling [8]-[10]. It enables the gate source voltage of certain MOS transistors to be adjusted with relation to the supply voltage.

The enhanced driving capability of transistors might lead to a decrease in latency and make it less vulnerable to process changes. To drive large capacitive loads with much reduced latency, the bootstrapped CMOS driver as described in [8] employs this technique. Each input transition triggers the bootstrapping procedure, however, since it is a static driver. According to [9], the conditional-bootstrapping latched CMOS driver suggests using conditional bootstrapping to cut down on redundant power use. Latched drivers like this one can only let you boost when the input and output logic values are at odds with one other. This increases energy efficiency by eliminating redundant boosting, especially in cases when there is minimal switching. A differential CMOS logic family that utilises the boosting technique has also been developed lately [10] for efficient operation in the near-threshold voltage region.

II. CONCEPTOF PROPOSED FLIP-FLOP FOR CONDITIONAL BOOSTING

There are four possible input data capture scenarios that need to be taken into consideration in order to include conditional boosting into a precharged differential flip-flop. These scenarios are based on the logic states of the input and output. The following are these scenarios:

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1) A high input should cause boosting to occur for a quick capture of incoming data if the output is low;
2) A low input should cause boosting to occur if the output is high since the input does not need to be captured;
3) A high input should cause boosting to occur for a quick capture of incoming data if it is low;
4) Ahigh output should cause a high input to cause no boosting.

By combining two operating principles, thesepossibilitiesmaybeimplementedinto a circuit design using a single boosting capacitor. One is that the data stored at the output (also known as output-dependent presetting) must be used to establish the voltage presetting for the boosting capacitor's terminals. The flip-flop's input data must provide the conditional basis for boosting operations (also known as input- dependent boosting). Fig. 1 displays the conceptual circuit diagrams that serve as evidence for these ideas.

As shown in Fig. 1(a), outputs Q and QB are used to calculate the preset voltages of capacitor terminals N and NB in order to facilitate output-dependent presetting. The noninverting input (D) is coupled to NB through a nMOS transistor, and the inverting input (DB) is coupled to N through an other nMOS transistor, as shown inFig.1(b).To support the input dependent boosting, N and NB are preset to be high and low if Q and QB are high and low, [left diagram in Fig. 1(a)]. Next, in one scenario where the flip-flop storeslowdata,which causesthe capacitor to preset as shown in the left diagram in Figure 1(a), a high input causes NB to be pulled to the ground, allowing N to be boosted towards –VDD as a result of capacitive coupling [upper left diagram in Figure 1(b)]. N may be connected to the ground in the meanwhile thanks to a low input, but since the node is already set to VSS, there is no voltage change at NB, therefore there is no boosting [bottom left schematic in Fig.1(b)].Allow input enables N to be dragged down to the ground, allowing NB to be boosted towards−VDD due to capacitive coupling [lower right diagram in Fig. 1(b)], similar to the opposite situation in which a high data is stored in the flip-flop, resulting in the capacitor presetting described in right diagram in Fig. 1(a).

Although the node is already set to VSS, a high input permits NB to be connected to the ground; nevertheless, this prevents any voltage change at N, which prevents boosting [upper right schematic in Fig. 1(b)].

To make these procedures simpler to grasp, Table I summarises them. These actions enable the removal of any unnecessary boosting, which significantly reduces power consumption, particularly when switching activity is minimal.

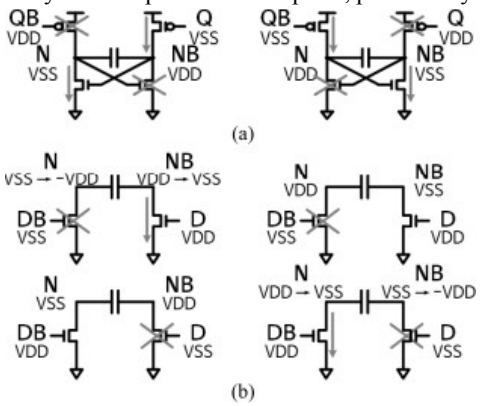

Fig. 1. Conceptual circuit diagrams for (a) output data-dependent presetting and (b) input data-dependent boosting

III. PROPOSED CIRCUIT IMPLEMENTATION

The proposed conditional-boosting flip-flop (CBFF) architecture, based on the concepts discussed before, is shown in Fig. 2. A symmetric latch, a conditional-boosting differential stage, and an explicit brief pulse generator make it up. In the conditional boosting differential stage shown in Fig. 2(a), MN5/MN6/MN7, equipped with boosting capacitor CBOOT, perform input-dependent boosting, while MP5/MP6/MP7 and MN8/MN9 handle output-dependent presetting. Figure 2(b) shows the symmetric latch as MP8–MP13 andMN10–MN15.

Figure 2(c) shows an example of an explicit pulse generator, which is a one-of-a-kind device for driving specific transistors in the differential stage with a brief pulsed signal PS. In contrast to conventional pulse generators, the proposed one does not include a pMOS keeper; this eliminates signal fighting when the PSB is being pushed down,

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resulting in quicker speed and lower power consumption. Coupled with MN1, MP1 acts as a keeper for the high logic value of PSB and also helps with the rapid pull-down of PSB.

At the rising edge of the CLK, MN1, MP1, and I1 rapidly discharge PSB, enabling PS to climb. Because MP2 charges PSB after I2 and I3 stall, PS drops back to a low state. As a result, the latency of I2 and I3 determines the breadth of the brief positive pulse at PS. When CLK is low, MP1 maintains a high PSB and disables MP2.

Based on our analysis, the energy savings may reach 9% while maintaining the same slew rate and pulse width.

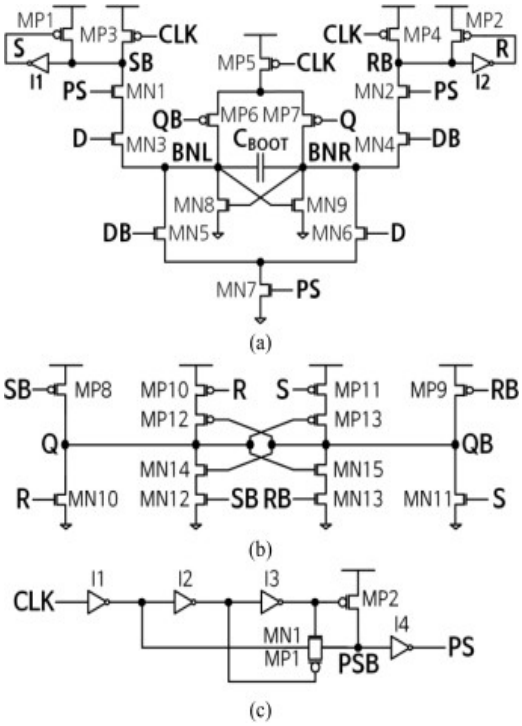

Fig. 2. Proposed CBFF. (a) Conditional- boosting differential stage. (b) Symmetric latch. (c) Explicit brief pulse generator.

IV. SIMULATED AND MEASURED RESULTS

It is recommended that you use CBFF in conjunction with other types of flip-flops, such as adaptive-coupling flip-flops (ACFFs) [6, SAFFs], differential skew tolerant flip-flops (STFF-Ds) [4, SCFFs) [5, and thoroughly]. It is possible to build and evaluate static topologically compressed flip-flops (TCFFs) [7] using a 65-nm CMOS technology. Another suggested flip-flop that is constructed and tested is the CBSF-SP, which uses a single explicit pulse generator shared by four main flip-flop circuits. The device size of every flip-flop is optimised to minimise EDP across all supply voltages. The output of every flip-flop is coupled with a 15 fF capacitive load.

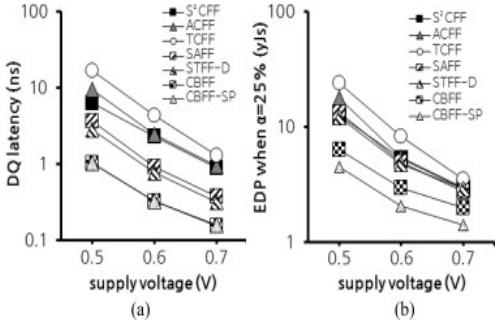

Fig. 3.Simulation resultsat various supply voltages. (a) DQ latency. (b) EDP.

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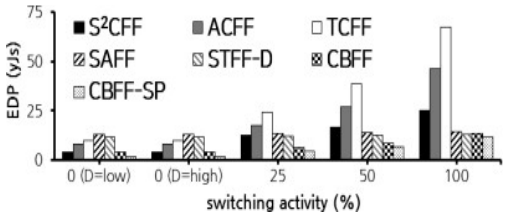

Fig.4.SimulatedEDPatvariousswitching activity conditions at 0.5 V.

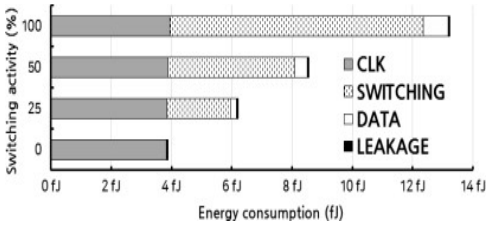

Fig. 5. Simulated energy of CBFF at 0.5V with various switching activities.

The boosting capacitor is implemented using a MOM capacitor. The suggested flip- flop's pulse width is chosen to provide sufficient margins to ensure data collection even in the most direction circumstances. The energy-delay product (EDP) and simulated data-to-output (DQ)latency of flip-flops at supply voltages between 0.5and0.7V.As, at 25% switching activity, CBFF outperforms SAFF and STFF-D by up to 72% and 63%, respectively, and has up to 53% and 47% lower EDPs. By sharing a pulse generator across many flip-flops, CBFFS Palsohas upto67%and63%lower EDPs[Fig.5(b)]than SAFF and STFF-Das well.

Due to their significantly high DQ latency, S2CFF, ACFF ,and TCFF perform worse in terms of EDP. The simulated EDP of flip- flopsat0.5Vsupply voltage in accordance with input switching activity. Because of conditional operation, the EDP improvements of CBFF and CBFF-SP over SAFF are as high as 70% and 85%, respectively. breaks down the power consumption of the suggested flipflop into its component parts, demonstrating how the switching power component reduces as switching activity does. to the boosting conditional. When switching is at zero, the clock circuit—which includes the pulse generator—consumes the bulk of the power. When the DQ latencies of flip-flops are compared with random process variation using a 1000-point Monte Carlo simulation, it becomes clear that the DQ latencies of CBFF and CBFF-SP are very resistant to process changes in the near- threshold voltage range. More specifically, compared to SAFF and STFF-D,CBFF has a DQ latency standard deviation that is 75%and85%lower,respectively.

Additionally, compared to SAFF and STFF-D,CBFF-SP has an EDP standard deviation that is 67% and 87% lower, respectively. We summarise the flipflop performance in Table II. The suggested flip-flops take up more layout space and need more gadgets. SinceS2CFF,ACFF,andTCFFare designed to be low power, their EDP performance is poor due to their high DQ latency and tiny energy consumption. Due to its pulsed operation, the suggested flip- flop has a comparatively long hold time; buffer stages at the output may be necessary to prevent hold time violations. Our analysis shows that buffer stages, which are used to prevent this problem, result in an approximate 7% EDP cost at 25% switching activity.

V. CONCLUSION

We provide a novel CBFF that aggressively scales voltages down to the near-threshold voltage range while maintaining considerable performance. An evaluation in a 25-nm CMOS process revealed that the proposed flip-flop is less vulnerable to process variation, has a lower EDP, and less DQ latency.

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