IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
Volume 2, Issue 3, November 2022
Impact Factor: 6.252

Design of Low Power 2-4 Mixed Logic Line Decoders

Smita Kumari[1] and Mr. Sandeep Kumar Dinkar[2]
PG Student, Laxmi Devi Institute of Engineering and Technology, Alwar, Rajasthan, India[1]
Assistant Professor, Laxmi Devi Institute of Engineering and Technology, Alwar, Rajasthan, India[2]
smitakumari25@gmail.com and sandinkar@gmail.com

Abstract: *This brief introduces a mixed-logic design method for line decoders, combining transmission gate logic; pass transistor dual-value logic, and static complementary metal-oxide semiconductor (CMOS). Two novel topologies are presented for the 2–4 decoders a 14 transistor topology aiming on minimizing transistor count and power dissipation and a 15transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. Furthermore, four new 4–16 decoders are designed by using mixed-logic2–4 pre decoders combined with standard CMOS post decoder. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulation sat 32 nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.*

Keywords: Low Power, 2-4 Mixed Logic, Line Decoders, CMOS, Transistor Topology

I. INTRODUCTION

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines or fewer if the n-bit coded information has unused combinations. The circuits examined here are n-to-m line decoders, which generate them = 2n minters of n input variables. Static cmos circuits are used for the majority of logic gates in integrated circuits. They consist of complementary N-type metal-oxide-semiconductor (n MOS) pull down and P type metal-oxide semiconductor (p MOS) pull up networks and present good performance as well as resistance to noise and device variation. Therefore, complementary metal-oxide semiconductor (CMOS) logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design. Pass transistor logic (PTL) was mainly developed in the 1990s, when various design styles were introduced, aiming to provide a viable alternative to CMOS logic and improve speed, power, and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual n MOS /p MOS pass transistors or parallel pairs of n MOS and p MOS called transmission gates. The most conventional one is complementary CMOS full adder (C-CMOS). It is based on regular CMOS structure with pull-up and pull-down transistors and has 28 transistors. Another conventional adder is the Complementary Pass Transistor Logic (CPL) with swing restoration which uses 32 transistors. CPL produces many intermediate nodes and their complement to make the outputs. The basic difference between the pass transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines. A Transmission Gate Full-Adder (TGA) presented in contains 20 transistors. Double pass transistor full adder cell has 48 transistors and operation of this cell is based on the double pass transistor logic in which both NMOS and PMOS logic networks are used. In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines or fewer if the n-bit coded information has unused combinations. The circuits examined here are n-to-m line decoders, which generate the m = 2n minters of n input variables In present scenario, power reduction is a

IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
Volume 2, Issue 3, November 2022
Impact Factor: 6.252

major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. The chip density and higher operating speed leads to the design of very complex chips with high clock frequencies. So, designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products. The development of electronic technology was started with the use of vacuum tube as active component in electronic series before semiconductor transistor replaces it. The development of microelectronic technology especially for those of mono-lyrical can produce interfaced circuit by combining all active and passive components in one chip. High speed serialize/deserializers (SerDes) are now more and more widely used in communication systems for serial interconnections.

II. DECODER

In digital systems, instructions as well as numbers are conveyed by means of binary levels or pulse trains. A decoder is a logic circuit that converts an N-bit binary input code into M output lines such that only one output line is activated for each one of the possible combinations of inputs. The decoder identifies or recognizes or detects a code. The N inputs can be a 0 or a 1, there are 2N possible input combinations or codes. For each of input combination only one of the M outputs will be active (HIGH), all other outputs will remain inactive (LOW). Some decoders are designed to produce active LOW output, while all the other outputs remain HIGH. In present scenario, power reduction is a major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. The chip density and higher operating speed leads to the design of very complex chips with high clock frequencies. So, designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products . The development of electronic technology was started with the use of vacuum tube as active component in electronic series before semiconductor transistor replaces it.

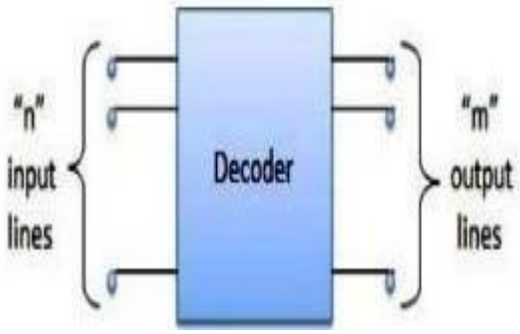

Figure 1: General Block diagram of decoder

The development of microelectronic technology especially for those of mono-litical can produce interfaced circuit by combining all active and passive components in one chip.High speed serialized/deserializes (SerDes) are now more and more widely used in communication systems for serial interconnections. Decoders are used whenever an output or a group of outputs is to activate only on the occurrence of specific combination of input levels. These input levels are often provided by the outputs of a counter or register. When the decoder inputs come from a counter that is being continually pulsed, the decoder outputs will be activated sequentially, and they can be used as timing or sequencing the signals to turn devices ON or OFF at specific times. Decoders are widely used in memory systems of computers, where they respond to the address code input from the central processor to activate the memory storage location specified by the address code. Low power consumption has been a priority and so pass transistor based tree decoders have been selected due to the lower leakage and dynamic switching currents. An asynchronous design would further help to reduce the dynamic power dissipation from the clock switching. Reliability has been the second important priority and design procedures for high read and write margins tolerant to process variations have been developed. Decoder In digital systems, instructions as well as numbers are conveyed by means of binary levels or pulse trains. A decoder is a logic circuit that converts an N-bit binary input code into M output lines such that only one output line is activated for each one of the possible combinations of inputs. The decoder identifies or recognizes or detects a code. The N inputs

IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
Volume 2, Issue 3, November 2022
Impact Factor: 6.252

can be a 0 or a 1, there are 2 N possible input combinations or codes. For each of input combination only one of the M outputs will be active (HIGH), all other outputs will remain inactive (LOW). Some decoders are designed to produce active LOW output, while all the other outputs remain HIGH [1]. Fig.1 General Block diagram of decoder III. 2-TO-4 DECODER In this paper, proposed 2-to-4 decoder with enable input is constructed with AND gates, it becomes more economical to generate the decoder output. A 2-to-4 decoder is enabled when E=1.The truth table of a 2-to-4 decoder is given in Table I and the general block diagram is shown in figure 2. The Boolean gate-based implementation of 2-to-4 decoder required four AND gates and two NOT logic gates.

III. LITERATURE SURVEY

R. Zimmermann and W. Fichtner, Jul.1997, Recently reported logic style comparisons based on full-adder circuits claimed complementary pass-transistor logic (CPL) to be much more power-efficient than complementary CMOS. However, new comparisons performed on more efficient CMOS circuit realizations and a wider range of different logic cells, as well as the use of realistic circuit arrangements demonstrate CMOS to be superior to CPL in most cases with respect to speed, area, power dissipation, and power-delay products. An implemented 32-b adder using complementary CMOS has a power-delay product of less than half that of the CPL version. Robustness with respect to voltage scaling and transistor sizing, as well as generality and ease-of-use, are additional advantages of CMOS logic gates, especially when cell-based design and logic synthesis are targeted. This paper shows that complementary CMOS is the logic style of choice for the implementation of arbitrary combinational circuits if low voltage, low power, and small power-delay products are of concern THE increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits.

K. Yano *et al.*, 1990. A 3.8-ns, 257-mW, 16*16-b CMOS multiplier with a supply voltage of 4 V is described. A complementary pass-transistor logic (CPL) is proposed and applied to almost the entire critical path. The CPL consists of complementary inputs/outputs, an nMOS passtransistor logic network, and CMOS output inverters. The CPL is twice as fast as conventional CMOS due to lower input capacitance and high logic functionality. Its multiplication time is the fastest ever reported, even for bipolar and GaAs ICs, and it can be enhanced further to 2.6 ns with 60 mW at 77 K.

M. Suzuki et al., 1993, A 32-b CMOS ALU (arithmetic and logic unit), fabricated using 0.25- mu m CMOS technology, that has a 1.5-ns addition time with a 2.5-V supply, is described. This addition time is achieved using double pass-transistor logic (DPL) and a conditional carry-selection (CCS) carry look-ahead circuit. The measured supply-voltage dependence of ALU addition time is shown, revealing excellent low-voltage performance. DPL AND/NAND and OR/NOR ring oscillators show measured speed improvements of 15% and 30% over CMOS NAND and NOR ring oscillators.

V. G. Oklobdzija and B. Duchene, 1995, New pass-transistor logic termed DVL which contains fewer transistors than its counterpart DPL yet maintain comparable performance. A method for synthesis of such networks is also developed and demonstrated in this paper. The new logic is characterized by good speed and low power. The simulations and tests were performed using 1 -pm ChrlOS New logic CMOS families using pass-transistor circuit techniques have recently been proposed with the objective of improving speed and power consumption. This logic (in most cases) passes the charge between the nodes rather than charging the nodes from VCC and then discharging them to GND. This feature contributes to less power being used as compared to the regular CMOS. The Double Pass-Transistor Logic (DIPL), developed by Hitachi demonstrated a 1.511s 32- bit ALU and 4.4nS 54-bit multiplier in 0.25 pm technology. However, DPL has not yet been fully adopted because of its high transistor count. The objective of the new logic gates and the synthesis method developed for pass-transistor logic is to minimize the number of transistors used in DPL and preserve the speed of the logic

IV. 2–TO-4 DECODER USING CMOS TECHNOLOGY

In this paper, a 2-to-4 Decoder has been designed to reduce power consumptionand surface area using 65nm, 45nm and 32nm complementary- metal- oxide semiconductor technology, which is then analysed and comparative study has been

IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
Volume 2, Issue 3, November 2022
Impact Factor: 6.252

donein account of the silicon surface area and power consumption. The proposed 2-to-4 Decoder using 32nm CMOS technology gives better results in terms of power and surface area as compare to 45nm and 65nm COMS technologies. The 2- to-4 decoder circuit size is 14.3 µm2 and typical power consumption is 0.172 µW at 32nm CMOS technology. Comparison of proposed 2-to-4 Decoder is based on the performance parameterslike surface area and power dissipation to achieve better performance using CMOS process by Micro wind 3.1 in 32nm, 45nm and 65nm technology. The proposed 2-to-4 Decoder circuit uses four 2-bit AND and two NOT logic gates.

V. LOW POWER CMOS FULL ADDERS USING PASS TRANSISTOR LOGIC

The efficiency of a system mainly depends on the performance of internal components present in the system. The internal components should be designed in such away that they consume low power with high speed. Lot of components is in circuits including full adder. This is mainly used in processors. A new Pass transistor full adder circuit is implemented in this paper. The main idea is to introduce the design of high performance and based pass transistor full adders which acquires less area and transistor count. The high performance of pass transistor low power full adder circuit is designed, and the simulation has been carried out on Tanner EDA Tool. The result shows that the proposed full adder is an efficient full adder cell with least MOS transistor count that reduces the high-power consumption and increases the speed. In this paper CMOS full adder circuits are designed to reduce the power and area and to increase the speed of operation in arithmetic application. To operate at ultra low supply voltage, the pass logic circuit that cogenerates the intermediate XOR and XNOR outputs has been improved to overcome the switching delay problem.

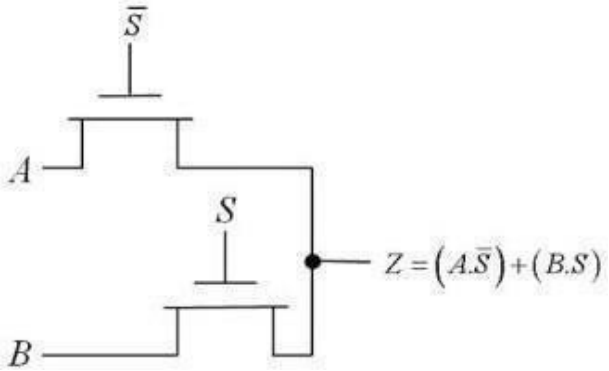

Figure 2: Design of a 2:1 MUX using pass-transistor logic

(i) Double-Pass Transistor Logic- Double-pass transistor logic eliminates some of the inverter stages required for complementary pass transistor logic by using both N and P channel transistors, with duallogical paths for each function. Though it has high speed due to low input capacitance, it has limited capacity to drive a load. The switching tree of a DPL gate consist of bothNMOS and PMOS pass transistors, in contrast to the switching tree of a CPL gate, usingonly NMOS transistors there. Full swing operation is attained by simply adding PMOStransistors in parallel with the NMOS transistors. However, this addition will result in increasing input capacitance. The switching tree of a CPL gate consists of only NMOS transistors, which results in a lower input capacitance. The fullswing output voltage restoration of a DPL-gate is done by the combination of an NMOS and a PMOS transistor, instead of the PMOS-latches and inverters which are used by means of Complementary Pass Transistor logic. Double pass transistor logic (DPL) uses both PMOS and NMOS devices in the pass-transistor network to avoid non full swing problems, but it has high-area and high-power drawbacks.

(ii) Pass Transistor Logic- In electronics, pass transistor logic (PTL) describes several logic families used inthe design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input.By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Since there is less isolation between input signals and outputs, designers must take care to assess the effects of unintentional paths within

IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
Volume 2, Issue 3, November 2022
Impact Factor: 6.252

the circuit. For proper operation, designrules restrict the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided. Simulation of circuits may be required to ensure adequate performance.

VI. CONCLUSION

This brief has introduced an efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS. By using this methodology, we developed fournew 2–4 line decoder topologies, namely 2–4LP, 2–4LPI, 2–4HP and 2–4HPI, which offer reduced transistor count and improved power delay performance in relation to conventional CMOS decoders. Furthermore, four new 4–16 line decoder topologies were presented, namely 4–16LP, 4–16LPI, 4–16HP and 4–16HPI, realized by using the mixed-logic 2-4 decoders as pre decoding circuits, combined with post decoders implemented in static CMOS to provide driving capability. A variety of comparative spice simulations was performed at 32 nm, verifying, in most cases, a definite advantage in favour of the proposed designs. The 2–4LP and 4–16LPI topologies are mostly suitable for applications where area and power minimization is of primary concern. The 2–4LPI, 2–4HP, and 2–4HPI, as well as the corresponding 4–16 topologies (4–16LP, 4–16HPI, and 4–16HP), proved to be viable and all-around efficient designs; thus, they can effectively be used as building blocks in the design of larger decoders, multiplexers, and other combinational circuits of varying performance requirements. Moreover, the presented reduced transistor count and low power characteristics can benefit both bulk CMOS and SOI designs as well. The obtained circuits are to be implemented on layout level, making them suitable for standard cell libraries and RTL design.

REFERENCES

[1] M Madhusudhan Reddy, Krishna Veni Challa, B Srinivasa Raja, "An Energy Efficient Static Address Decoder for High-Speed Memory Applications", 2022 7th International Conference on Communication and Electronics Systems (ICCES), pp.50-53, 2022.
[2] Alok Kumar Mishra, Shubham Sinha, D.D.V Subbarao, D. Vaithiyanathan, Baljit Kaur, "Study and Implementation of Low Power Decoder using DVL and TGL Logic", 2021 IEEE Madras Section Conference (MASCON), pp.1-6, 2021.
[3] Aarchi Jain, Anshuman Singh, Smita Singhal, Aditya Mudgal, Anu Mehra, "A Novel Power Efficient 2:4 Decoder at 16nm", 2021 International Conference on Computer Communication and Informatics (ICCCI), pp.1-4, 2021.
[4] Anuradha C. Ranasinghe, Sabih H. Gerez, "MEPNTC: A Standard-Cell Library Design Scheme Extending the Minimum-Energy-Point Operation of Near-V_{th} Computing", 2020 IEEE 38th International Conference on Computer Design (ICCD), pp.96-104, 2020.
[5] Vazgen Sh Melikyan, Kamo O. Petrosyan, Artur Kh. Mkhitaryan, Hayk V. Margaryan, "The Method Of Low Power, High Performance And Area Efficient Address Decoder Design For SRAM", 2020 IEEE 40th International Conference on Electronics and Nanotechnology (ELNANO), pp.276-279, 2020.
[6] Rohit Kumar Arya, Sonali Agrawal, "Design of Efficient 2–4 Modified Mixed Logic Design Decoder", 2019 International Conference on Communication and Electronics Systems (ICCES), pp.29-34, 2019.
[7] N S Sumana, B Sahana, Abhay A Deshapande, "Design and Implementation of Low Power - High Performance Mixed Logic Line Decoders", 2019 4th International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT), pp.529-534, 2019.
[8] Ayushee Sharma, "Optimizing Power and Improving Performance of 4-16 Hybrid-Logic Line Decoder using Power Gating Technique", 2019 4th International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT), pp.510-513, 2019.
[9] B. Jeevan, K. Sivani, "A Review on different Logic Styles to design High Performance VLSI Decoders", 2018 International Conference on Networking, Embedded and Wireless Systems (ICNEWS), pp.1-6, 2018.
[10] Chaitanya Kommu, A. Daisy Rani, "A New High-Performance 4-Bit Code Converter and Parity Checker Using Mixed Logic Design", Journal of Circuits, Systems and Computers, vol.31, no.05, 2022.
[11] Venkata Krishna Odugu, Venkata Narasimhulu C, Satya Prasad K, "An efficient VLSI architecture of 2□D finite impulse response filter using enhanced approximate compressor circuits", International Journal of Circuit Theory and Applications, vol.49, no.11, pp.3653, 2021.