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A Comparative Performance Analysis of CMOS XOR XNOR Circuits

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Abstract: *New XOR-XNOR circuit modes are proposed to improve speed and power as these circuits are the building blocks of multiple arithmetic circuits. This project evaluates and compares the performance of various XOR-XNOR circuits. The performance of XOR-XNOR circuits is tested by comparing the simulation results obtained with Electric VLSI. The mimicry results show which region has the lowest PDP and EDP performance, the most energy efficient and fastest compared to the best available XOR-XNOR circuits.*

Keywords: Exclusive-OR (XOR), Exclusive-NOR (XNOR), High Speed, Low Power, Arithmetic Circuits. Circles

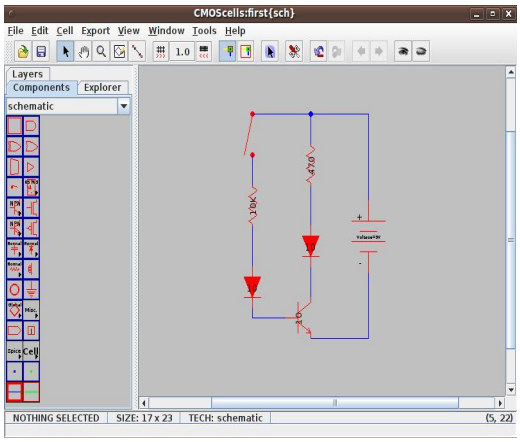
I. INTRODUCTION

While the growth of the electronics market has propelled the VLSI industry to a much higher integration and system in chip-building and more than a few GHz operating frequencies, key concerns have always arisen from the huge increase in energy consumption and the need to further reduce them. In addition, with the growing growth in demand and popularity of portable electronics drive designers are pushing for less silicon space, higher speed, longer battery life, and more reliability. Power is one of the premium resources a designer tries to conserve when designing a system

1.1 Software Used

The Electric VLSI Design System is an EDA tool originally written 1980s by Steven M. Rubin. Electricity is used to create logic wire scematics and to perform an integrated circuit structure analysis.
It can also manage hardware definitions such as VHDL as well Veriloge Program has many analytical and integration tools, including Exploring Design Law, Simulation, Route, Structure vs. Schematic, Logical Effortt and so on. Electric is written in Java, and released as part of the GNU project in 1998 under the GNU General Public License. In 2017, power upgrades ceased, but support and bug fixes continued.

1.2 Front End of Electric 9.7



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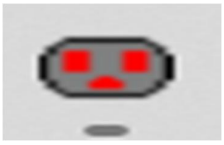
1.3 Symbol of Electric 9.7



LTspice

LTspice is a computer-based analog electronic circuit simulator computer software, developed by semiconductor manufacturer Analog Devices (originally Linear Technology). SPICE software that is widely distributed and widely used in the industry. Although Freeware LTspice is not limited to hypocrisy to limit its power (no feature limits, no node limits, no component limits, no subcircuit limits). t sends through the library of SPICE models from Analog Devices, Linear Technology, Maxim Integrated, and third-party sourcesProblem formulation:-

This project aims to "Comparative study of performance parameters of XOR XNOR circuits. The XOR and XNOR circuit is used for pass transistor logic, CMOS logic station, transmission gate logic. Due to the low power consumption and high speed these design circuits are suitable for arithmetic operations and VLSI applications. Comparison of delays and strengths are therefore found in various design strategies for sensible gates

II. REVIEW OF VARIOUS XOR AND XNOR CIRCUIT DESIGN OF DIFFERENT CMOS LOGIC STYLES

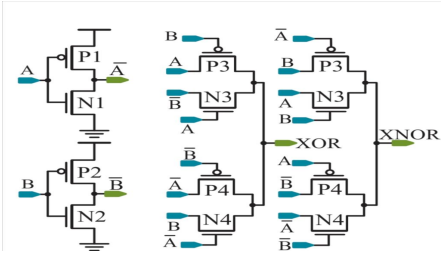


Fig.(a)

Figure (a) shows the fully enclosed XOR / XNOR gate circuit designed in the style of double pass-transistor logic (DPL). This building has eight transistors. The main problem with this circuit is to use two high power NO gates on the key circuit circuit, because NO gates have to drive the output power. Therefore, the size of the transistors in the NO gates should be increased to obtain the minimum delay of the critical path. In addition, it causes the formation of a centralized node with high potential. Of course, this means that NO gates drive out of the circuit, for example, pass a transistor or TG. So, short-circuit power too, so, the total power dissipation of this circuit is greatly increased. Moreover, in the best case scenario of the PDP, the delays in the critical process will also increase slightly.

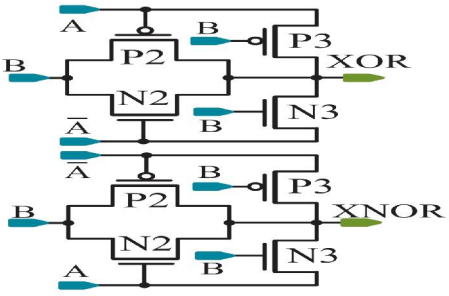


Fig.(b)

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Figure (b) shows another example of a fully equipped XOR / XNOR gate, each made up of six transistors. This cycle is based on the PTL logical style, your delays and power consumption are better than the cycles shown in Fig. (a). The only problem with this building is the use of NO gates in the main path of the circuit. XOR circuit of Fig. 1 (b) has a lower delay than its XNOR circuit, due to the fact that the key line of the XOR circuit is made up of NO gates with nMOS transistor (N3). But the main route of the XNOR circuit includes NO gates and pMOS transistor (P5) (pMOS transistor is slower than nMOS transistor). Therefore, in order to improve the speed of the XNOR circuit, the size of the pMOS transistor (P5) and NOT gates must be increased.

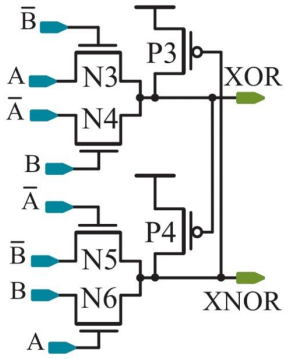

Fig.(c)

Figure (c) shows an example of the XOR – XNOR circuit at the same time. This cycle is based on the CPL style designed using ten transistors. In this structure, the output is driven only by the nMOS transistor, therefore, two pMOS transistors are connected to the output (XOR and XNOR) as integrated couplings to restore the output capacity. One problem with this XOR – XNOR circuit is that it has a feedback (cross-linked structure) output, which increases the delay and power of this short circuit. Therefore, in order to reduce the set delay, the size of the transistors should be increased. Another disadvantage of this building is the presence of two gates NOT on the critical road.

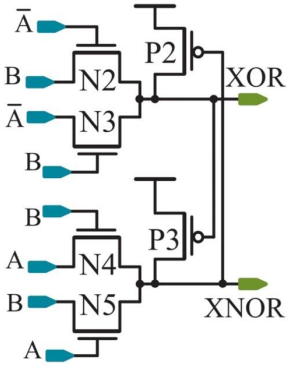

Fig.(d)

In Fig. (d), if the input is AB = 00, transistors N3, N4, and N5 are closed and logic "0" is transferred to transistor N2 to XOR output. This “0” in XOR charges XNOR output to VDD via transistor P3. Therefore, the critical pathway of this region is greater than that of the Fig. Cycle. (c). Also, in this structure, the short-circuit current will be transferred to the circuit where the input is converted from AB = 01 to AB = 00. When the input is in AB = 01, logic "1" is transmitted through transistors. N2, N3, and P2 to XOR output and logic "0" are transferred to transistor N4 to XNOR output. If the input changes to AB = 00, all transistors will be switched off except transistors N2 (input A) and P2 (with XNOR output, which has not changed now). Therefore, the current-circuit current will pass through transistors P2 and N2.

If the current value found in transistor P2 is greater than the current immersion in transistor N2, the short-circuit current will continue to be drawn to VDD and will not change the output of XOR and XNOR. This situation also occurs when the input is changed from AB = 11 to AB = 10 and affects the efficiency of the circuit. In order to provide optimal

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performance for this circuit, the ON-state resistance of transistors P2 and P3 should not be less than that of transistors N2 and N5 (RP2> RN2, RP3> RN5), respectively. In addition, this structure is highly sensitive to diversity processing; if the size of the transistors is changed, the circuit may not function properly

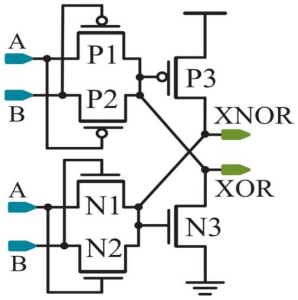

Fig.(e)

The proposed XOR – XNOR gate with six transistors is proposed [shown in Fig. (e)]. Two parallel response transistors (N3 and P3) return weak memory to output nodes (XOR and XNOR) when input equal to AB = 00, 11. However, this circuit suffers from severe case delays, because if the input changes from AB = 01, 10 to AB = 11, 00, the results reach their final electrical value in two steps. To clarify the problem, when input equal to AB = 10, the logic "1" and the logic "0" pass through the transistors of N2 (XOR) and P2 (XNOR output), respectively. By changing the input mode to AB = 11, transistors P1 and P2 are closed (XOR node initially high impedance) and weak logic "1" (VDD-Vthn) is transmitted via transistors N1 and -N2 exit XNOR. Weak logic "1" in XNOR OPENS N3 response so that XOR output is subtracted with a weak "0," this weak logic "0" opens P3 response. Finally, a constructive response is made and the results of XNOR and XOR will have a strong logic "1" and a logic "0," respectively. This slow response problem is worse for low voltage performance and increases short-circuit current [when single output (XOR or XNOR) is a high delay and circuit response is not fully operational, short-circuit current passes. through the circuit].

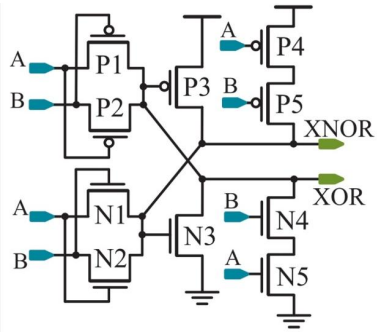

Fig. (f)

In the cycle of Fig. (f), in order to solve the slow reaction problem and utilize the low power supply, two nMOS transistors (AB = 11) and two pMOS transistors (AB = 00) added to XOR and XNOR. results, respectively. The advantages of this structure are good driving strength, fullswing output, and durability against transistor sizing as well as providing voltage scaling. A major problem with this circuit is the response structure that places additional parasitic forces on the XOR and XNOR output nodes. Therefore, delays and energy consumption increase significantly.

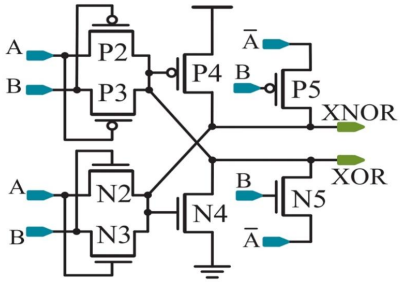

Fig.(g)

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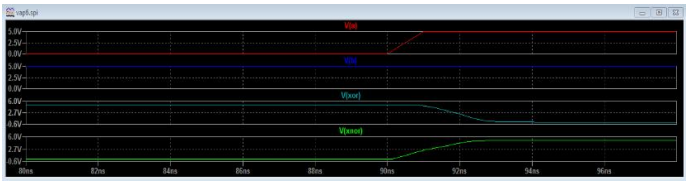
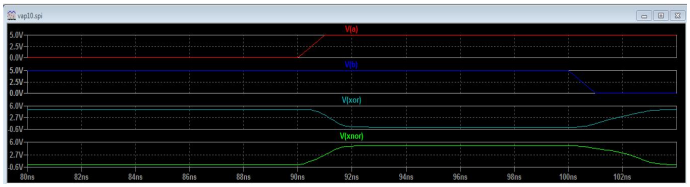
Figure (g) shows another region for the development of Fig. Structure. (e). In this structure, NO gate is used to improve rotational speed. This cycle has better speed than Fig. (e), because in Fig. (g), transistors N5 and P5 have a route from GND or VDD to output nodes in two input regions (AB = X1 in N5 and AB = X0 for P5). But in Fig. (e), transistors N4 and P5 have the same modes for only one input mode (AB = 11 on N4 and AB = 00 on P5). Also, with the addition of the NO gate, a central node with a large capacitance will be built that will increase the power consumption of the circuit. Therefore, Fig. (g) has more power consumption than figure (e). A combination of the two XOR and XNOR circles of Fig. (a) and (b) will result in two simultaneous levels of XOR – XNOR. These new structures will have all the advantages and disadvantages of their XOR / XNOR circuits

III. RESULT

Comparison of outputs having 6 transistors and 10 transistors in Xor-Xnor cell





Comparison of Circuits implemented

Circuit Logic	No of Transistors	Cell Area	Delay	Max. Load Current
Double pass transistor	12	2769	4.5nS	770uA
Pass transistor	10	1352	6nS	595uA
Cross Coupled PMOS	8	3264	4ns	890uA
Complementry Feedback	6	1368	3nS	610uA
Improvement in Complementry Feedbac	10	3370	2nS	680uA

IV. APPLICATION

1. ADDER design
2. Multiplier Design
3. Compressor design

V. CONCLUSION

Also, with the addition of the NO gate, a central node with a large capacitance will be formed which will increase the power consumption of the circuit. Therefore, Fig. (g) has more power consumption than figure (e). A combination of the two XOR and XNOR circles of Fig. (a) and (b) will result in two simultaneous levels of XOR - XNOR. These new facilities will have all the advantages and disadvantages of their XOR / XNOR circuits

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