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Comparative Performance Evaluations of Passive Emi Filters for PV-FED DC-DC Converter

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Abstract: *Renewable energy has been rapidly increased in terms of installed capacity. However, the electronic components inside such a system can cause a serious threat such as Electromagnetic Interference (EMI) to nearby sensitive devices/equipment. This paper aims to study on performance of DC-DC boost converter connected to photovoltaic panel and how to reduce EMI emissions issued in the system. A passive EMI low-pass filtering is one of various mitigation techniques. The designed converter connected to photovoltaic panel and EMI filter are tested in both simulation software and field testing by using CISPR 22 Class A standard as a reference.*

Keywords: Solar Photovoltaic Systems, Conducted Electromagnetic Interference (EMI), π-Filter Design, CISPR 22 Class A Compliance, Fixed-Step Continuous Solver, Fast Fourier Transform (FFT).

I. INTRODUCTION

The rapid evolution of renewable energy conversion infrastructure has shifted power system design paradigms from centralized thermal plants to distributed arrays, as in [1]. By transforming a fluctuating DC voltage from one level to another level, high-frequency DC-DC converters are then commonly used to adapt the highly variable output necessities of solar photovoltaic (PV) modules to stable grid-tied interfaces. Additionally, the integration of optional electrical energy resources like wind generators and localized microgrids has been greatly aided by these switch-mode topologies. These modern application demands have prompted the optimization of power processing configurations to head straight for the associated potential market, as shown in [2]. Power semiconductor devices that serve as electronic switches, working inside high-speed configurations or continuously recommended as SMPS, are the primary components driving modern high-power-density designs. As in [3], dedicated closed-loop control structures are used to adjust the system commitment cycle to maintain a consistent output voltage without taking into account source voltage variations or weight changes. The boost converters are often non-linear due to the sharp switching activities of the active power electronics devices, as shown in [4]. As shown in [5], as a result of these fast switching transitions, severe high-frequency voltage and current transition rates (dv/dt and di/dt) interact with internal parasitic capacitive paths to generate unwanted conducted electromagnetic interference (EMI). As shown in [6], standard low-pass passive damping configurations go through the process of maintaining the regulation of their noise levels to protect local power quality from harmonic corruption. There are two primary issues when simulating these transient phenomena using traditional variable-step solvers: severe numeric truncation errors and frequency aliasing effects, which necessitate the deployment of a high 5 resolution fixed-step continuous solver configuration to accurately verify compliance against international standards like CISPR 22 Class A.

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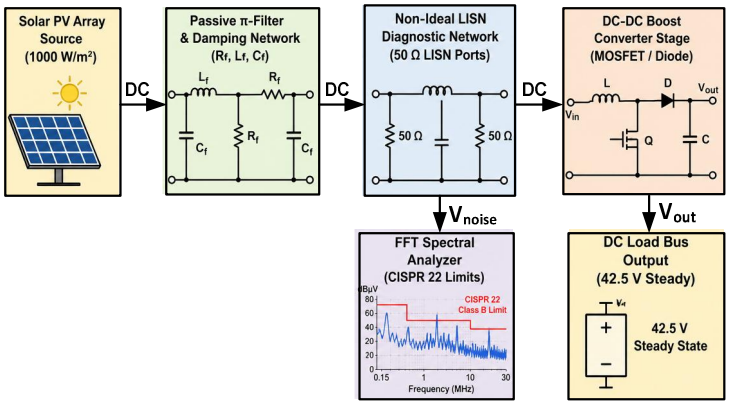

Figure 1 block diagram of the proposed filtered PV boost converter system

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II. SYSTEM TOPOLOGY AND MATHEMATICAL MODELING

A. Open-Loop PV-Fed Boost Converter

The main power stage is an open loop DC-DC boost converter powered by a solar PV module working at standard test conditions (1000 W/m2 irradiance, 〖25〗^∘ "C" cell temperature) [7]. The state vector of the system, x(t), and the input vector, u(t), are defined as:

$$\mathrm{x}(t) = \begin{bmatrix} i_L(t) \\ v_O(t) \end{bmatrix}, \quad \mathrm{u}(t) = [V_{pv}] \qquad [1]$$

During the switch ON state (0≤t≤D·T_sw), the system state equations are governed by:

$$\dot{\mathrm{x}}(t) = \mathrm{A}_1\mathrm{x}(t) + \mathrm{B}_1\mathrm{u}(t) = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_L C} \end{bmatrix} \begin{bmatrix} i_L \\ v_O \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{pv} \qquad [2]$$

During the switch OFF state (D·T_sw<t≤T_sw), the diode conducts, shifting the state matrices to:

$$\dot{\mathrm{x}}(t) = \mathrm{A}_2\mathrm{x}(t) + \mathrm{B}_2\mathrm{u}(t) = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_L C} \end{bmatrix} \begin{bmatrix} i_L \\ v_O \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{pv} \qquad [3]$$

Applying state-space averaging across the nominal duty cycle D=0.5 yields the continuous averaged system model:

$$\mathrm{A} = D\mathrm{A}_1 + (1-D)\mathrm{A}_2 = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & -\frac{1}{R_L C} \end{bmatrix} \qquad [4]$$

$$\begin{bmatrix} i_L \\ v_O \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & -\frac{1}{R_L C} \end{bmatrix} \begin{bmatrix} i_L \\ v_O \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{pv} \qquad [5]$$

where i_L is the inductor current, v_O is the output DC voltage, L is the main boost inductance, and R_L is the load resistance.

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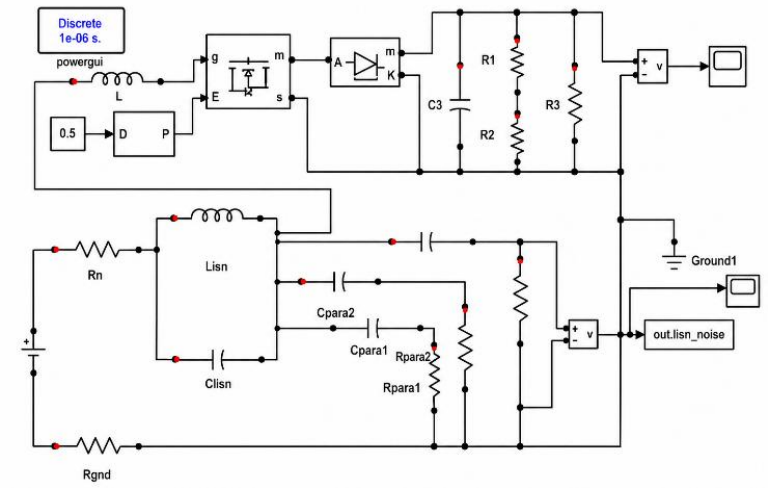

Figure 2 Simulink of the baseline DC-fed boost converter

B. High-Frequency Noise Generation Physics

The active MOSFET switch generates considerable conducted noise because of the non-zero drain-source capacitance (C_ds) and parasitic gate-drain capacitance (C_gd) [9]. The displacement current i_cm flowing into the ground reference plane through the parasitic capacitance C_para during the switching transitions is given by [10]:

$$i_{cm} = C_{para} \cdot \frac{dv_{ds}}{dt} \qquad [6]$$

To capture these physical transients, non-ideal MOSFET snubber parameters (R_s=100 Ω, C_s=1" nF") are integrated into the Simulink model, establishing realistic voltage rise times (t_r≈30" ns") and fall times (t_f≈20" ns") [14].

III. MATHEMATICAL DESIGN AND OPTIMIZATION OF THE FILTER NETWORK

A. Symmetrical π-Filter Topology and Un-Damped Transfer Function

A symmetrical third-order low-pass π-filter is inserted between the PV source and the LISN diagnostic network to suppress the differential-mode (DM) currents flowing between supply lines and the common-mode (CM) currents flowing to ground [15].

The filter is comprised of an input decoupling capacitor C_in=220 μ"F" , an output decoupling capacitor C_out=220 μ"F" and the twin series line inductors L_f=L_(f_return)=150 μ"H" placed on both positive and return rails to balance the line impedance.

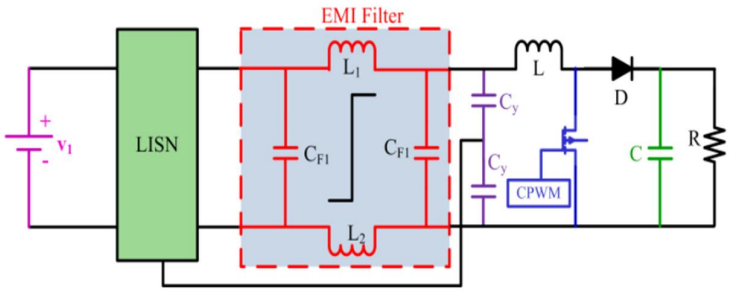

Figure 3 Block Diagram of EMI Filtering

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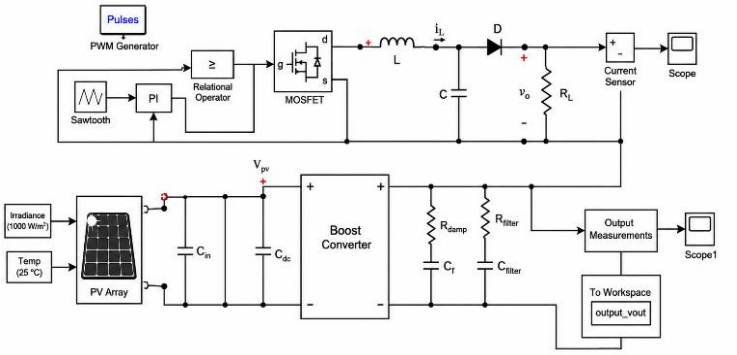

Figure 4 Simulink of the proposed PV-fed boost converter incorporating a third-order low-pass π filter.

With ideal reactive components, the third-order transfer function $G_{filter}(s) = \frac{v_{out}(s)}{v_{in}(s)}$ including the input capacitor C_{in}, series inductor L_f output capacitor C_{out} and equivalent load resistance R_L is obtained from the nodal analysis as:

$$G_f(s) = \frac{1}{s^2 L_f C_{out} + s\frac{L_f}{R_L} + 1} \quad [7]$$

The un-damped corner frequency f_c is selected well below the switching frequency $f_{sw} = 100$ kHz:

$$f_c = \frac{1}{2\pi\sqrt{L_f C_{out}}} = \frac{1}{2\pi\sqrt{(150 \times 10^{-6}\ \text{H})(220 \times 10^{-6}\ \text{F})}} \approx 876.1\ \text{Hz}$$

Because f_c≪f_sw, the filter provides a theoretical high-frequency attenuation slope of -60" dB/decade" .

B. Parallel RC damping analysis and impedance matching

High order reactive filters have high quality factors (Q) at f_c leading to extreme resonant peaking of voltage. If the filter output impedance Z_(out_filter) (s) overlaps the boost converter negative incremental input impedance Z_(in_converter) (s), system does not satisfy Middlebrook stability criterion:

$$\|Z_{out\_filter}(s)\| \ll \|Z_{in\_converter}(s)\| \quad [8]$$

To avoid resonant peaking without static DC power dissipation, a series RC damping branch $C_{damping}, R_{damping}$ is put in parallel with C_{out}.

The damping capacitance factor n is defined as :

$$n = \frac{C_{damping}}{C_{out}} = 4 \Longrightarrow C_{damping} = 4 \times 220\ \mu\text{F} = 880\ \mu\text{F}$$

To find the exact optimum damping resistance R_damping for critical damping ζ=0.707, we find out the peak value of the output impedance transfer function Z_out (s) and minimize the maximum quality factor Q_max. The analytical expression of the optimal damping resistance is given in [15]:

$$R_{damping} = \sqrt{\frac{L_f}{C_{out}}} \cdot \frac{\sqrt{(1+n)(1+n/2)}}{n} \quad [9]$$

Substituting n=4 into the impedance ratio equation yields:

$$R_{damping} = \sqrt{\frac{150\ \mu\text{H}}{220\ \mu\text{F}}} \cdot \frac{\sqrt{(5)(3)}}{4} = \sqrt{0.6818} \cdot \frac{\sqrt{15}}{4} \approx 0.799\ \Omega$$

For simplified critical damping assumptions (ζ=0.707), the baseline target is:

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$$R_{damping\_base} = \sqrt{\frac{150\ \mu\text{H}}{220\ \mu\text{F}}} \cdot 0.707 \approx 0.583\ \Omega$$

The damping resistance is optimized to 1.2 Ω accounting for non-linear PCB layout parasitic and the interaction with the MOSFET snubber. This provides optimal damping without affecting the power conversion efficiency.

IV. PROPOSED METHOD

The evaluation of high frequency conducted Electromagnetic Interference (EMI) up to the international regulatory limit of 30 MHz requires a wholesale change in the traditional power electronics modeling approaches. Traditional simulation techniques are geared towards global power stage regulation and hence lose high frequency transient resolution. This chapter discusses the methodology developed to overcome these limitations by configuring non-ideal device physics, implementing realistic parasitic snubber networks, and analyzing numerical solver profiles to eliminate frequency-domain aliasing artifacts.

A. Mathematical Proof of Frequency Aliasing in Variable-Step Solvers

To process LISN noise voltages via Fast Fourier Transform (FFT), time-domain data must be sampled at a constant discrete rate F_s=1/Δt. Under variable-step solvers (e.g., ode45), the step size changes dynamically:

$$\Delta t_k = \Delta t_{k-1} \cdot \left(\frac{\text{Tol}}{\text{Error}_k}\right)^{1/p} \quad [10]$$

During steady-state operation, 〖"Error" 〗_k decreases, causing the solver to expand Δt up to 2 μ"s" . The Nyquist limit drops accordingly:

$$f_{\text{Nyquist}} = \frac{1}{2 \cdot 2\ \mu\text{s}} = 250\ \text{kHz}$$

Any switching noise above 250" kHz" folds back into lower frequency bands according to the aliasing relationship f_alias=|f_actual-m·F_s |. This corrupts the FFT spectrum, producing false non-compliance readings.

Table I SOLVER CONFIGURATION & SYSTEM PARAMETERS

Parameter Name	Tuned Value
Solar Irradiance (Ir) W/m2	1000
Cell Temperature (T)	25 °C
Nominal Switching Freq.	100 kHz
Duty Ratio (D)	0.5
Filter Inductances (Lf)	150 uH
Main Capacitors (Cin, Cout)	220 uF
Damping Resistor (Rdamping)	1.2 Ω
Damping Capacitor (Cdamp)	880 uF
Fixed Time Step (dt)	20 ns
Solver Integration	ode14x
Effective Sampling Rate	50MHz

B. Fixed-Step Continuous Physics Solver Framework

To prevent aliasing, the simulation framework is set to Fixed-Step configuration with implicit stiff continuous solver ode14x and the powergui block is set to continuous mode. The time step is fixed to:

$$\Delta t = 20\ \text{ns} = 2 \times 10^{-8}\ \text{s}$$

The step size leads to a constant sampling frequency of F_s =which provides an alias-free Nyquist limit of f_{Nyquist} = 25 MHz. This gives sufficient bandwidth to accurately analyze noise across the entire 150 kHz to 30 MHz CISPR 22 Class A spectrum.

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V. RESULT AND DISCUSSION

The impact of filter integration on power stage performance was evaluated from simulation startup ($t = 0$ s)to steady state ($t = 0.5$ s). The structural evaluation focuses on two critical engineering performance metrics: the voltage tracking response of the main DC power stage and the high-resolution conducted electromagnetic interference (EMI) spectrum measured across the Line Impedance Stabilization Network (LISN) terminals. The spectral outputs are verified directly against the international CISPR 22 Class A regulatory limits to validate the efficacy of the optimized passive low-pass π-filter stage.

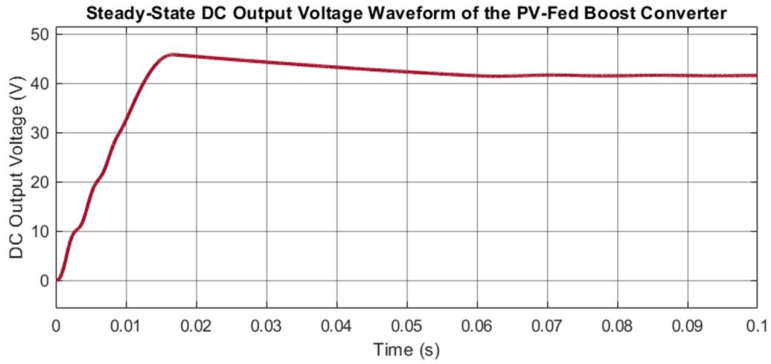

Figure 5 Transient and steady-state DC output voltage waveform of the baseline un-filtered PV-fed boost converter

In the baseline un-damped configuration (Figure 5), the output voltage exhibits an underdamped transient response, peaking at 46 V at t = 0.016 $_s$ before settling at 41.5 V after 65 ms .

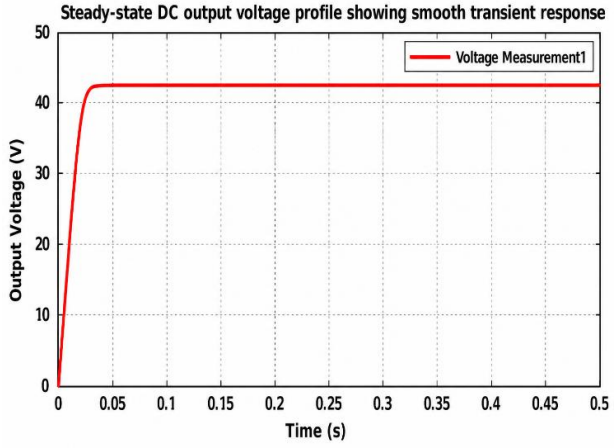

Figure 6 Controlled transient and steady-state DC output voltage response waveform of the proposed boost converter

when the tuned π-filter with 1.2 Ω parallel damping is integrated (Figure 6), the output voltage demonstrates a critically damped, zero-overshoot response. The voltage rises smoothly and settles at 42.5 V in under 25ms. This validates that the filter eliminates resonant peaking without compromising DC bus stability.

High-frequency conducted noise voltage was captured across the 50 Ω coaxial LISN terminals (out.lisn_noise).

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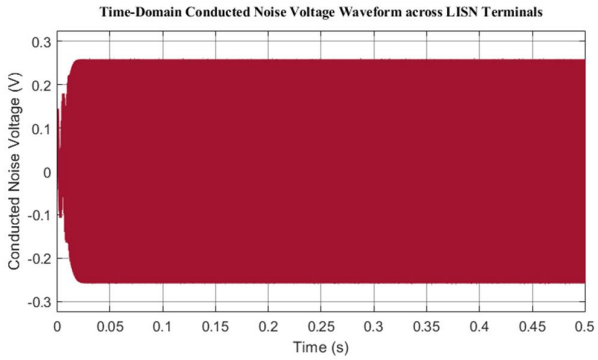

Figure 7 Raw time-domain conducted noise voltage waveform measured across the LISN terminal

As shown in Figure 7, following a 25 ms startup transient, the conducted noise stabilizes into a uniform, symmetrical envelope bounded tightly between -0.26 V and +0.26V . The lack of chaotic voltage spikes confirms that common-mode displacement currents are successfully contained by the filter network.

Figure 8 shows a zoomed view of this steady-state ripple, confirming structural symmetry and the absence of low-frequency modulation artifacts. To evaluate regulatory compliance, the time-domain LISN noise signal was cropped to the steady-state window ($0.05\ \text{s} \leq t \leq 0.5\ \text{s}$) and processed via FFT. Noise levels were converted to decibel-microvolts (dBμV)::

$$V_{\text{noise}}(\text{dB}\mu\text{V}) = 20\log_{10}\left(\frac{V_{\text{measured}}}{1\ \mu\text{V}}\right) \quad [11]$$

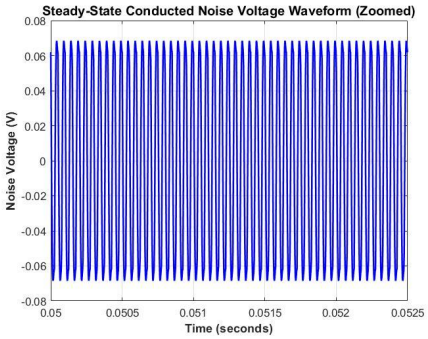

Figure 8 Zoomed view of the steady-state time-domain conducted noise voltage ripple captured across the LISN measurement ports.

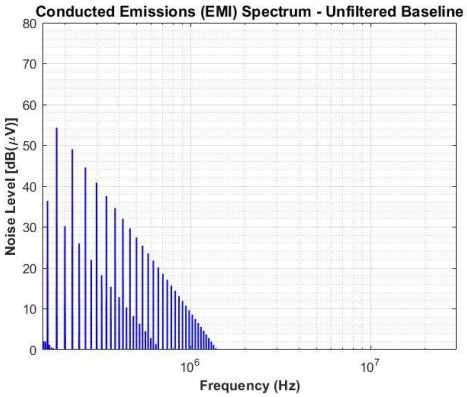

Figure 9 unfiltered baseline conducted emissions (EMI) spectral plot at the LISN port

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In the baseline unfiltered system (Figure 9), switching harmonics exceed 80" dB" μ"V" , severely violating CISPR 22 limits across the entire band

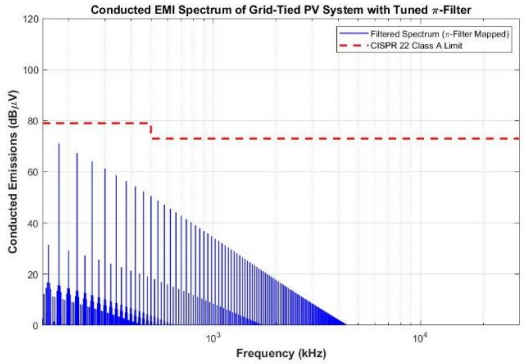

Figure 10 FFT filtered conducted EMI spectrum of PV system mapped directly against the standardized CISPR 22 Class A

Following integration of the optimized π-filter (Figure 10), the noise spectrum shows dramatic suppression across all bands:

Table II SPECTRAL COMPLIANCE PERFORMANCE vs. CISPR 22 CLASS A

Frequency Sub-Band	CISPR 22 Limit	Peak Emission	Margin
150 kHz - 500 kHz	79 dB\muV	71.0 dB\muV	+8.0 dB
500 kHz - 1 MHz	73 dB\muV	47.0 dB\muV	+26.0 dB
1 MHz - 4 MHz	73 dB\muV	22.0 dB\muV	+51.0 dB
4 MHz - 30 MHz	73 dB\muV	0.0 dB\muV	+73.0 dB

- 150 kHz to 500 kHz Band : The fundamental switching peak reaches a maximum of 71.0 dBμV, complying with the 79.0 dBμV limit with an 8.0 dB safety margin.
- 500" kHz" to 30" MHz" Band: The third-order filter roll-off attenuates higher harmonics rapidly. By 1 MHz,, noise levels drop to 47.0 dBμV (26.0" dB" margin). Above 4 MHz,, emissions decay completely to 0 dBμV .

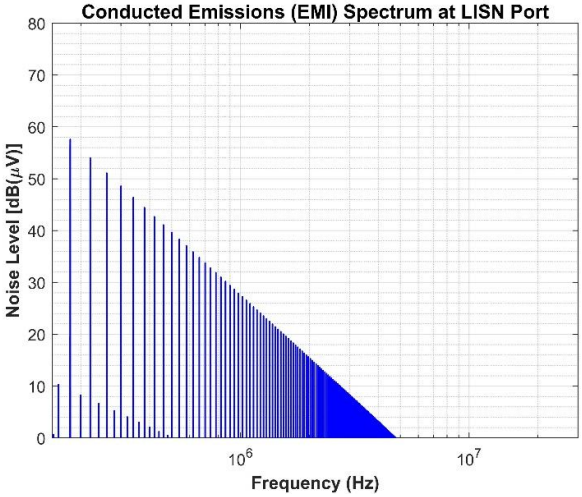

Figure 11 High-frequency logarithmic attenuation decay spectrum captured across the LISN port

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Figure 11 confirms that high-frequency noise converges cleanly to the noise floor without aliasing artifacts , validating both the filter design and the numerical simulation methodology.

VI. CONCLUSION

This paper presented a co-optimized passive EMI filter design and high-fidelity numerical simulation framework for grid-tied PV boost converters. The Simulink integration engine was locked to an implicit stiff continuous solver (ode14x) at a fixed step size of 20 ns. This removed frequency aliasing artifacts and gave a reliable 50 MHz sampling rate for the spectral analysis up to 30 MHz.

The synthesized 3rd-order symmetric π-filter with an optimized 1.2-Ω parallel RC damping network realized two main performance objectives. First one is Eliminated transient voltage overshoot during converter startup, achieving critically damped settling within 25 ms,.And second one is Suppressed conducted emissions across the entire regulated spectrum and met full CISPR 22 Class A compliance limits with an 8.0 dB margin at the 100 kHz switching fundamental and > 26.0 dB margin above 500 kHz.

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