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Neuromorphic Computing: From Device Physics to Scalable Systems – A Comprehensive Review

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Abstract: *Neuromorphic computing has emerged as a promising paradigm for addressing the growing energy demands of modern computing by incorporating brain-inspired principles into physical hardware. However, a major challenge lies in scaling individual synaptic devices from laboratory demonstrations to integrated systems capable of real-world applications. This review examines recent progress from device-level innovations to system-level architectures and standardized benchmarking frameworks. In particular, it discusses emerging implementations of artificial synapses based on spintronic and photonic technologies, including photoresponsiveheterostructures and optical scattering techniques that exploit intrinsic physical phenomena for information processing. At the device scale, mechanisms such as magnetic switching, optical response, and wave interference enable efficient and parallel computation. Translating these devices into practical neuromorphic systems requires overcoming integration challenges related to device interconnectivity, power management, and compatibility across heterogeneous platforms, including photonic and electronic circuits. Furthermore, the development of standardized benchmarking frameworks is crucial for evaluating performance, comparing architectures, and identifying system limitations. This review consolidates recent advances in device physics, neuromorphic architectures, and evaluation methodologies, highlighting key directions for the development of scalable and energy-efficient neuromorphic computing systems beyond conventional architectures.*

Keywords: Neuromorphic Computing, Spintronic Synapses, Photonic Neural Networks, Neuromorphic Hardware, Benchmarking Frameworks, Energy-Efficient Computing.

I. INTRODUCTION

The fast growth of intelligence and deep learning has put a lot of pressure on the computers we use today. These new neural networks need more power to work and the cost of energy to train and use them on regular computers is getting too high. This is why people are looking for ways to build computers that can work well without using too much energy.

Neuromorphic computing is a way to solve this problem by looking at how the brain works. Of keeping memory and processing separate like regular computers do neuromorphic computers combine these functions in the hardware. This means they can work with power and only do things when they need to. The idea of computing was first talked about by Carver Mead in the 1980s. Since then it has become an area of research that includes many fields, like how devices work, circuit design, system architecture and making algorithms [1]. Despite significant progress, there is still a major gap between early device-level demonstrations and the creation of scalable, real-world systems. While researchers have successfully developed artificial synapses and neurons using various technologies, turning these individual components into fully integrated systems that can match the performance of conventional hardware is still a challenge.

Another issue is the lack of standard evaluation methods. Because different research groups use different ways to measure performance, it becomes difficult to fairly compare results across platforms. This makes it harder to clearly understand which approaches are most effective and ready for practical deployment. [2]. This review observes the

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current state of neuromorphic computing through a device-to-system lens, covering spintronic and photonic implementations of artificial synapses, considers to scaling neuromorphic architectures, and the role of benchmarking frameworks in advancing the field toward maturity.

II. SPINTRONIC SYNAPSES AND NEURONS

Spintronic offers a physically rich substrate for neuromorphic hardware, exploiting magnetic phenomena such as non-linearity, hysteresis, phase transitions, and non-volatility to implement synaptic and neuronal functions natively in hardware. Unlike purely electronic approaches, spintronic devices can combine memory and computation within a single element, aligning well with the requirements of neuromorphic systems.

Artificial synapses must store analogue weight information and update it in response to incoming signals. Magnetic tunnel junctions (MTJs) represent one of the most mature spintronic technologies for this purpose. While standard MTJs are binary devices, analogue behaviour can be achieved through domain wall motion within the free magnetic layer, allowing a continuous range of resistance states. This memristive behaviour mirrors the potentiation and depression mechanisms of biological synapses.Beyond domain wall devices, skyrmion-based synapses have attracted attention due to topological stability and low driving currents. Simulations have shown that the number of skyrmions in a magnetic chamber can encode synaptic weight, with current pulses driving skyrmions into or out of the active region to modulate the weight value. Spintronic neurons exploit magnetic dynamics to replicate leaky integrate-and-fire (LIF) behaviour. Repeated input current pulses gradually shift a magnetic state toward a threshold, beyond which the device fires and resets. Spin-torque nano-oscillators are particularly well suited to this role. At the network level, spoken digit recognition benchmarked at 99.6% accuracy on the NIST TI-46 corpus has been achieved using time-multiplexed spin-torque oscillator reservoirs [3,4].

III. PHOTONIC AND OPTICAL IMPLEMENTATIONS

Photonic platforms offer complementary advantages in terms of bandwidth, parallelism, and potential for passive, energy-free linear computation. Integrated photonic networks can perform matrix-vector multiplication with minimal propagation losses, making them attractive for the linear processing layers of neural networks.

Wanjura and Marquardt proposed that a fully nonlinear neuromorphic system can be constructed using only linear wave scattering. By encoding the network input into the physical parameters of a linear scattering system rather than into the probe signal itself, the resulting input-output relationship becomes nonlinear through the structure of the scattering matrix. This was validated on handwritten digit recognition, achieving 97.1% accuracy, and implemented on racetrack resonator arrays. A distinct approach is the reconfigurable all-optical synaptic device based on an IGZO/SnO/SnSheterostructure. This device integrates sensing, storage, and processing within a single optoelectronic element. Both excitatory and inhibitory synaptic behaviours can be induced using light stimulation across ultraviolet and visible wavelengths without external voltage modulation. An 8×8 synaptic array demonstrated image perception and memory functions, achieving 91% accuracy on handwritten numeral recognition [5].

IV. SCALING NEUROMORPHIC SYSTEMS

Moving from individual devices to functional systems at scale introduces distinct challenges. Kudithipudi et al. define neuromorphic computing at scale as the capacity of a system to operate at the size, speed, and energy required for complex real-world tasks. Key architectural features include sparsity in neural activity and connectivity, distributed and hierarchical organization, and asynchronous communication protocols.

The progression from early perceptron circuits to Intel Loihi 2 with 1.15 billion neurons and SpiNNaker2 with 5.2 billion neurons illustrates the field's trajectory [4]. Hardware and software co-design is identified as critical, as the diversity of platforms means algorithms are often hardware-dependent, limiting portability and slowing progress.

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V. BENCHMARKING FRAMEWORKS

Neuromorphic hardware has evolved from small experimental systems to highly scalable, brain-inspired architectures with massive neuron counts. Early systems like Perceptron had only a few hundred neurons. From the 2000s onward, systems rapidly scaled to millions and billions of neurons. Modern platforms such as SpiNNaker2 and Loihi 2 reach billion-scale neurons. The upward highlights exponential growth, indicating rapid advancement toward brain-scale computing.

The absence of standardized benchmarks has been one of the most significant obstacles to progress. NeuroBench addresses this through a dual-track framework covering algorithm-level and system-level evaluation. The algorithm track provides hardware-independent benchmarks across tasks including few-
shot continual learning, event camera object detection, motor cortical signal decoding, and chaotic time series prediction.

Baseline results demonstrate consistent efficiency advantages: Loihi 2 requires 37 times less power than a CPU solver on optimization tasks, and Xylo consumes 60 times less dynamic inference power than an Arduino on acoustic scene classification [2].

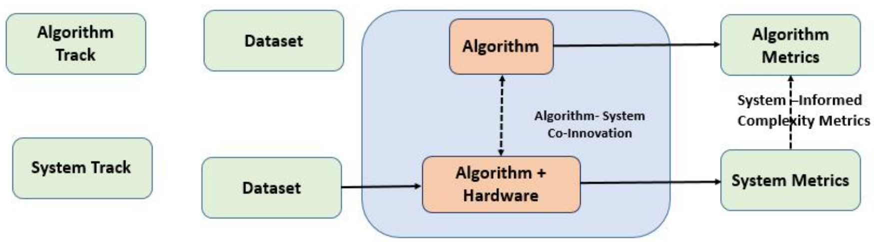

Fig. 1. NeuroBench two-track framework for neuromorphic evaluation [5].

VI. CONCLUSION

Neuromorphic computing stands at an important juncture. Spintronic and photonic implementations have demonstrated artificial synapses and neurons across a range of physical substrates. Recent work has begun to address the architectural requirements for scaling these devices into practical platforms, and standardized benchmarking frameworks mark a further step toward rigorous, reproducible evaluation. The path forward requires tighter integration across the full stack from device physics through system architecture, algorithm development, and evaluation methodology pointing toward a future where neuromorphic hardware offers a genuinely competitive alternative to conventional computing for energy-constrained applications.

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