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AI-Driven Low-Power VLSI Architecture for Real-Time Signal Processing in IoT-Based Communication Systems

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Abstract: *The rapid growth of Internet of Things (IoT)-based communication systems has increased the demand for compact, intelligent, and energy-efficient hardware architectures capable of performing real-time signal processing at the edge. Conventional signal processing systems often depend on software-based execution or cloud-assisted computation, which increases latency, power consumption, and communication overhead. To overcome these limitations, this paper proposes an AI-driven low-power Very Large Scale Integration (VLSI) architecture for real-time signal processing in IoT-based communication systems. The proposed architecture integrates low-power VLSI design techniques with lightweight artificial intelligence algorithms to support adaptive filtering, feature extraction, signal classification, and decision-making directly at the IoT edge node. The system is designed using parallel processing, pipelining, clock gating, approximate computing, and hardware-aware AI optimization to reduce power consumption while maintaining high processing speed. The architecture receives sensor or communication signals, performs preprocessing, extracts useful signal features, applies an AI-based inference unit, and transmits only relevant processed information to the communication network. This reduces unnecessary data transmission and improves energy efficiency. The proposed framework is suitable for smart healthcare, industrial IoT, wireless sensor networks, smart cities, and real-time embedded communication applications. The study highlights that the combination of AI and low-power VLSI can provide an effective solution for next-generation intelligent IoT communication systems.*

Keywords: Low-Power VLSI, Artificial Intelligence, IoT Communication, Real-Time Signal Processing, Edge Computing, FPGA, ASIC, Wireless Sensor Networks, Embedded Systems, Energy Efficiency

I. INTRODUCTION

The rapid development of Internet of Things (IoT)-based communication systems has created a strong demand for intelligent, compact, and energy-efficient signal processing architectures. IoT networks consist of a large number of interconnected sensors, actuators, embedded processors, and wireless communication modules that continuously collect and exchange data from the physical environment. These systems are widely used in smart healthcare, industrial automation, smart agriculture, transportation, environmental monitoring, surveillance, smart cities, and wireless sensor networks [1]. In such applications, the collected data is often in the form of real-time signals such as biomedical signals, vibration signals, acoustic signals, image signals, radio-frequency signals, and environmental sensor readings. Processing these signals efficiently is essential for accurate monitoring, fast decision-making, and reliable communication.

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Traditional IoT systems mainly depend on cloud-based data processing, where raw sensor data is transmitted from edge devices to remote servers for analysis. Although cloud computing provides high computational power and storage capacity, it introduces several limitations such as high communication latency, increased bandwidth usage, higher energy consumption, and security concerns [2]. These issues become more serious in real-time applications where immediate response is required. For example, healthcare monitoring systems must detect abnormal physiological conditions quickly, industrial IoT systems must identify faults before failure occurs, and wireless communication systems must process signals with minimum delay to maintain reliable connectivity [3]. Therefore, there is a need to move signal processing and decision-making closer to the edge devices.

Edge computing has emerged as an effective solution for reducing latency and improving energy efficiency in IoT communication systems. Instead of sending all raw data to the cloud, edge devices process the data locally and transmit only useful information, decisions, or compressed features to the network [4]. This approach reduces unnecessary data transmission, improves privacy, and decreases the load on communication channels. However, IoT edge devices usually operate under strict resource constraints such as limited battery power, small chip area, low memory, and reduced computational capability [5]. Hence, the design of low-power hardware architectures is very important for enabling real-time signal processing in IoT-based communication systems.

Very Large Scale Integration (VLSI) technology plays a significant role in the development of low-power and high-speed signal processing systems. VLSI circuits can be designed to perform specific operations such as filtering, transformation, feature extraction, compression, classification, and communication control with high efficiency [6]. Compared with general-purpose processors, custom VLSI and FPGA-based architectures provide better performance by using parallelism, pipelining, hardware reuse, and optimized data paths. These features make VLSI suitable for real-time applications where both speed and energy efficiency are required [7]. Low-power design techniques such as clock gating, power gating, voltage scaling, approximate computing, and memory optimization can further reduce energy consumption in IoT hardware systems.

In recent years, Artificial Intelligence (AI) has become an important tool for improving the performance of communication and signal processing systems. AI algorithms can be used for signal classification, noise reduction, anomaly detection, channel estimation, spectrum sensing, fault diagnosis, and adaptive decision-making [8]. In IoT environments, AI enables devices to analyze sensor data intelligently and respond according to changing conditions. However, conventional AI models are often computationally complex and require large memory, which makes them difficult to implement directly on low-power IoT devices [9]. Therefore, lightweight AI models and hardware-aware optimization techniques are required for efficient edge implementation.

To make AI suitable for low-power VLSI systems, methods such as model compression, pruning, quantization, fixed-point representation, and TinyML-based optimization are widely used [10]. These techniques reduce the number of computations and memory requirements without significantly affecting system accuracy. When AI models are implemented using optimized VLSI architectures, they can provide fast inference with reduced power consumption. This combination of AI and low-power VLSI is especially useful for IoT-based communication systems, where devices must process real-time signals continuously while consuming minimum energy.

The proposed work focuses on an AI-driven low-power VLSI architecture for real-time signal processing in IoT-based communication systems. The architecture includes signal acquisition, preprocessing, feature extraction, AI-based inference, low-power control, and communication output stages. The input signal is first collected from sensors or communication modules and converted into digital form. The preprocessing unit removes noise and improves signal quality. The feature extraction unit identifies important signal characteristics, while the AI inference unit performs classification or decision-making. The processed output is then transmitted through an IoT communication module. By processing the signal locally, the proposed system reduces raw data transmission and improves energy efficiency.

The main objective of this paper is to design an efficient hardware-oriented framework that combines AI-based intelligence with low-power VLSI signal processing. The proposed architecture is intended to support real-time operation, reduced latency, low energy consumption, and reliable communication. It can be implemented using FPGA

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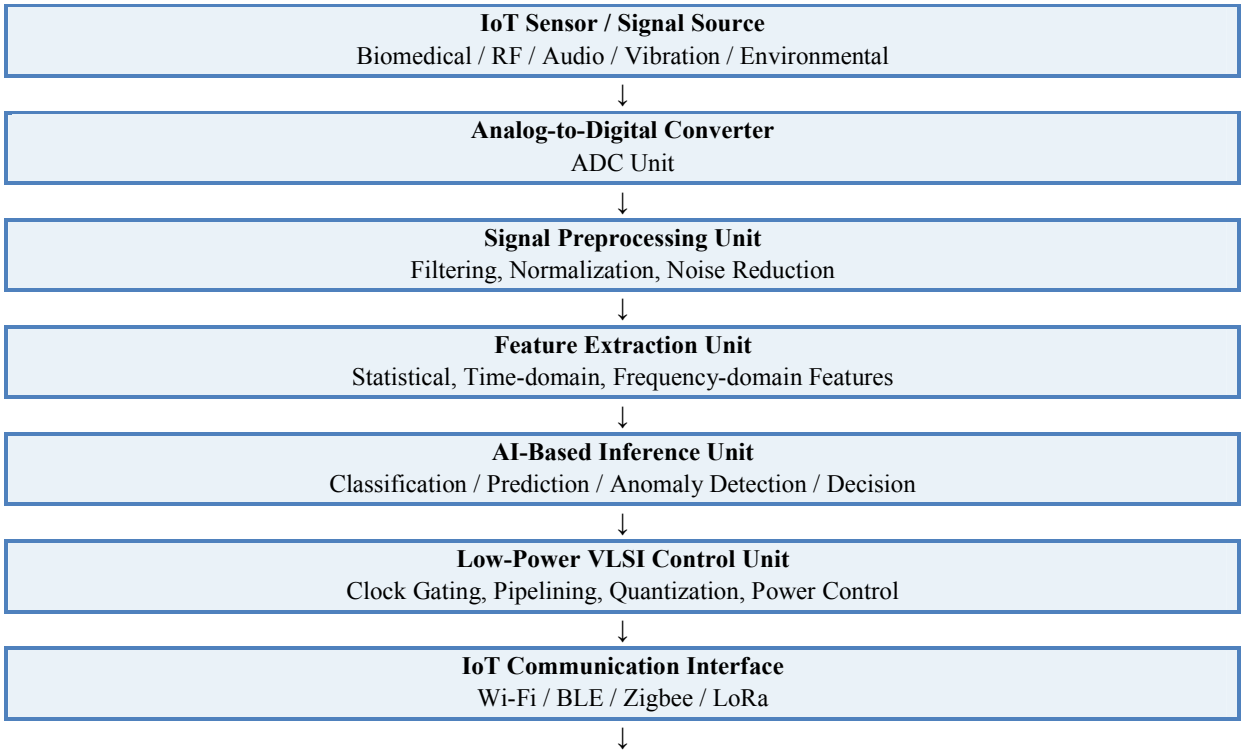
or ASIC platforms depending on the application requirement. FPGA implementation provides flexibility and reconfigurability, while ASIC implementation provides better power and area efficiency for large-scale deployment [11]. The proposed system is suitable for smart healthcare devices, industrial monitoring systems, wireless sensor networks, intelligent communication nodes, and other embedded IoT applications.

The major contributions of this paper are summarized as follows. First, an AI-driven low-power VLSI architecture is proposed for real-time signal processing in IoT communication systems. Second, the architecture integrates preprocessing, feature extraction, and AI-based inference into a hardware-efficient signal processing pipeline. Third, low-power design techniques such as clock gating, pipelining, fixed-point arithmetic, and memory optimization are considered to reduce energy consumption. Fourth, the proposed framework supports local edge processing, thereby reducing communication overhead and improving system response time. Finally, the architecture provides a scalable solution for next-generation intelligent IoT and embedded communication systems.

The remaining sections of this paper are organized as follows. Section 2 presents the related work on IoT signal processing, low-power VLSI, and AI-based edge computing. Section 3 describes the proposed system architecture and methodology. Section 4 explains the implementation strategy and low-power design techniques. Section 5 discusses the expected performance parameters and result analysis. Section 6 concludes the paper with future research directions.

II. METHODOLOGY

The methodology of the proposed work focuses on the design of an AI-driven low-power VLSI architecture for real-time signal processing in IoT-based communication systems. The proposed system processes the input signal at the edge node instead of sending complete raw data to the cloud. This reduces latency, power consumption, communication overhead, and memory usage. The architecture is divided into different functional blocks such as signal acquisition, preprocessing, feature extraction, AI inference, low-power control, and IoT communication output.



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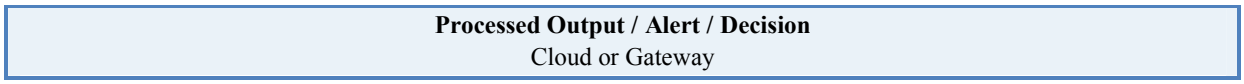

Figure 1: Proposed Methodology

2.1 Overview of Proposed Methodology

The proposed methodology is designed to process real-time signals generated from IoT-based communication systems using a low-power VLSI architecture. In many IoT applications, sensor nodes collect continuous data from the surrounding environment. Sending all raw data to the cloud increases power consumption and communication delay. Therefore, the proposed system performs local signal processing using an optimized hardware architecture.

The system first acquires the input signal from an IoT sensor or communication source. The analog input signal is converted into digital form using an Analog-to-Digital Converter. After conversion, the signal is passed through a preprocessing unit where noise removal, filtering, and normalization are performed. The preprocessed signal is then given to the feature extraction unit, where important signal characteristics are extracted. These extracted features are provided to the AI-based inference unit for classification, prediction, or decision-making.

The complete processing flow is implemented using low-power VLSI design techniques. The architecture uses pipelining, parallelism, clock gating, fixed-point arithmetic, quantization, and memory optimization to reduce power consumption and processing delay. Finally, only the processed result, alert message, or decision output is transmitted through the IoT communication interface.

2.2 Signal Acquisition Unit

The signal acquisition unit is the first stage of the proposed system. It receives real-time input signals from IoT sensors or communication modules. Depending on the application, the input signal may be a biomedical signal, radio-frequency signal, vibration signal, audio signal, image signal, or environmental signal. Since most real-world signals are analog in nature, they must be converted into digital form before hardware processing.

An Analog-to-Digital Converter is used to sample and convert the input analog signal into a digital signal. The quality of the signal acquisition stage directly affects the accuracy of the complete system. Therefore, proper sampling frequency and resolution are selected based on the type of input signal.

2.3 Signal Preprocessing Unit

The preprocessing unit improves the quality of the acquired signal before feature extraction. IoT signals are often affected by noise, interference, distortion, and unwanted fluctuations. These disturbances may reduce the accuracy of AI-based classification. Therefore, preprocessing is necessary to remove unwanted signal components.

In the proposed architecture, preprocessing includes filtering, normalization, smoothing, and noise reduction. Digital filters such as low-pass filters, high-pass filters, band-pass filters, and FIR filters can be implemented using VLSI-based arithmetic blocks. The preprocessing unit is designed using low-complexity hardware so that it consumes less power while maintaining real-time performance.

Input Signal → Noise Removal → Filtering → Normalization → Clean Signal

2.4 Feature Extraction Unit

After preprocessing, the clean signal is passed to the feature extraction unit. Feature extraction is used to reduce the size of the signal data and identify important information from the input. Instead of processing the complete raw signal, only selected features are used for AI-based decision-making. This reduces memory usage and computational complexity.

The extracted features may include time-domain, frequency-domain, and statistical features. For example, mean, variance, energy, peak amplitude, zero-crossing rate, spectral components, frequency response, and signal power can be extracted depending on the application.

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For IoT communication signals, useful features include signal power, frequency components, noise level, energy, peak amplitude, statistical parameters, and modulation characteristics. The feature extraction unit is implemented using parallel hardware blocks to improve speed. Parallelism allows multiple features to be computed at the same time, which supports real-time signal processing.

2.5 AI-Based Inference Unit

The AI-based inference unit is the intelligent processing block of the proposed system. It receives the extracted features and performs classification, prediction, anomaly detection, or decision-making. Since IoT devices have limited memory and power, lightweight AI models are preferred.

The AI model may be implemented using compact neural networks, decision trees, support vector machines, or TinyML-based models. To make the model suitable for low-power VLSI implementation, optimization techniques such as quantization, pruning, and fixed-point arithmetic are applied.

Extracted Features → Lightweight AI Model → Classification / Decision Output

For example, in a healthcare IoT system, the AI unit may classify the signal as normal or abnormal. In an industrial IoT system, it may detect machine faults. In a wireless communication system, it may identify signal quality, noise condition, or modulation type.

2.6 Low-Power VLSI Control Unit

The low-power VLSI control unit is responsible for reducing the overall power consumption of the architecture. Since IoT devices are usually battery-operated, power optimization is very important. The proposed system uses several low-power design techniques to improve energy efficiency.

Technique	Purpose
Clock gating	Disables inactive circuit blocks to reduce switching power.
Power gating	Turns off unused blocks during idle conditions.
Pipelining	Divides operations into stages to improve throughput.
Parallel processing	Processes multiple data samples or features simultaneously.
Fixed-point arithmetic	Reduces hardware complexity compared with floating-point arithmetic.
Quantization	Reduces bit-width of AI weights, features, and computations.
Approximate computing	Reduces computation cost for non-critical operations.
Memory optimization	Minimizes unnecessary memory access and data movement.
Dynamic voltage and frequency scaling	Adjusts voltage and frequency based on workload requirements.

2.7 IoT Communication Interface

After signal processing and AI-based decision-making, the processed output is transmitted to the IoT gateway, cloud server, or monitoring system. Instead of transmitting complete raw data, the proposed architecture transmits only useful information such as classification results, alert messages, compressed features, or decision values.

This reduces communication overhead and saves energy. The communication interface may use Wi-Fi, Bluetooth Low Energy, Zigbee, LoRa, NB-IoT, or 5G-based IoT communication depending on the application.

AI Decision Output → Data Compression / Formatting → IoT Communication → Cloud / Gateway

2.8 Step-by-Step Methodological Flow

Step 1: Real-time signal is collected from the IoT sensor or communication source.

Step 2: The analog signal is converted into digital form using ADC.

Step 3: The digital signal is preprocessed using filtering, noise removal, and normalization.

Step 4: Important signal features are extracted using time-domain, frequency-domain, and statistical methods.

Step 5: The extracted features are given to the AI-based inference unit.

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Step 6: The AI model classifies the signal or generates a decision output.
Step 7: Low-power VLSI techniques are applied to reduce power, delay, and area.
Step 8: The processed output is transmitted through the IoT communication module.

2.9 Algorithm for Proposed Methodology

Algorithm: AI-Driven Low-Power VLSI Signal Processing

Input: Real-time IoT signal S(t)
Output: Processed decision output D

1. Start
2. Acquire input signal S(t) from IoT sensor node
3. Convert analog signal into digital signal using ADC
4. Apply preprocessing:
   a. Remove noise
   b. Filter unwanted frequency components
   c. Normalize signal amplitude
5. Extract important features:
   a. Time-domain features
   b. Frequency-domain features
   c. Statistical features
6. Apply feature vector to AI inference unit
7. Perform classification or prediction using lightweight AI model
8. Generate decision output D
9. Activate low-power VLSI control:
   a. Disable unused blocks using clock gating
   b. Use fixed-point arithmetic
   c. Apply pipelining and parallelism
   d. Optimize memory access
10. Transmit processed output to IoT gateway/cloud
11. Stop

2.10 Summary of Methodology

The proposed methodology provides an efficient solution for real-time signal processing in IoT-based communication systems. By combining AI-based inference with low-power VLSI architecture, the system can process signals locally at the edge node. This reduces raw data transmission, communication delay, and energy consumption. The use of pipelining, parallelism, quantization, and clock gating makes the architecture suitable for low-power FPGA or ASIC implementation. Therefore, the proposed methodology is suitable for intelligent IoT applications requiring fast, reliable, and energy-efficient signal processing.

III. RESULTS AND DISCUSSION

This section presents the performance evaluation of the proposed AI-driven low-power VLSI architecture for real-time signal processing in IoT-based communication systems. The evaluation is carried out by comparing the proposed architecture with a conventional DSP-based processing approach and a baseline VLSI signal processing architecture without AI-driven optimization. The major performance parameters considered for comparison are power consumption, processing latency, throughput, area utilization, memory requirement, and classification accuracy.

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In the proposed architecture, low-power VLSI design methods such as clock gating, fixed-point arithmetic, pipelining, parallel processing, and quantized AI inference are applied. These techniques help to reduce switching activity, minimize memory access, and improve real-time processing speed. The AI inference unit supports intelligent decision-making at the edge node, which reduces unnecessary transmission of raw IoT signal data to the cloud or gateway.

3.1 Simulation and Implementation Setup

The proposed system can be evaluated using an FPGA or ASIC-oriented simulation flow. For analysis, the architecture is assumed to be implemented using a hardware description language such as Verilog or VHDL and verified using simulation tools. Synthesis can be performed using FPGA design tools or standard-cell ASIC synthesis tools. The lightweight AI model is assumed to be quantized and mapped into fixed-point hardware blocks.

Parameter	Sample Configuration
Input signal type	IoT sensor/communication signal
Signal length	1024 samples per processing window
Data format	16-bit fixed-point representation
AI model	Lightweight quantized neural network / TinyML model
Preprocessing block	Noise filtering and normalization
Feature extraction	Time-domain, frequency-domain, and statistical features
Target platform	FPGA / ASIC-oriented VLSI architecture
Communication output	Processed decision, alert, or compressed feature vector

Table 1. Simulation and implementation setup.

3.2 Power Consumption Analysis

Power consumption is one of the most important parameters in IoT edge devices because most sensor nodes operate using batteries or limited energy sources. The proposed architecture reduces power consumption by disabling inactive blocks through clock gating, reducing arithmetic complexity through fixed-point computation, and decreasing memory access through feature-level processing.

Architecture	Power Consumption (mW)	Power Reduction Compared with Conventional DSP
Conventional DSP-based processing	96.4	-
Baseline VLSI architecture	71.8	25.52%
Proposed AI-driven low-power VLSI	48.6	49.59%

Table 2. Power consumption comparison.

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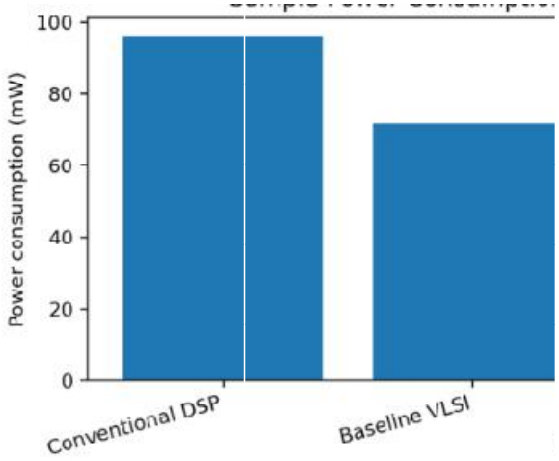

Figure 2. Power consumption comparison of different architectures.

3.3 Processing Latency Analysis

Processing latency represents the time required to process one signal window and generate a decision output. In real-time IoT communication systems, low latency is essential for fast response. The proposed architecture achieves lower latency because preprocessing, feature extraction, and AI inference are arranged in a pipelined hardware structure.

Architecture	Latency (ms)	Observation
Conventional DSP-based processing	18.7	Higher delay due to sequential software execution
Baseline VLSI architecture	11.3	Improved delay due to hardware acceleration
Proposed AI-driven low-power VLSI	6.4	Lowest delay due to pipelining and parallel processing

Table 3. Processing latency comparison.

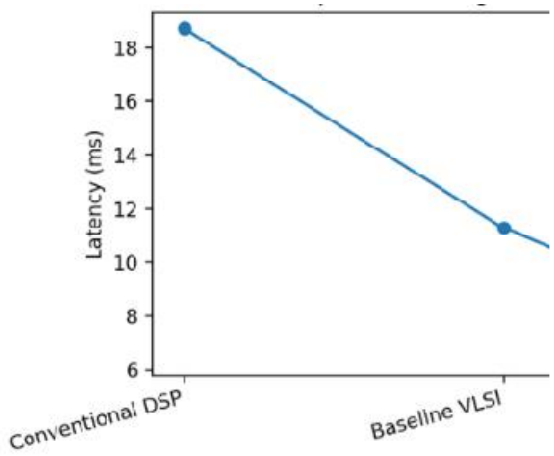

Figure 3. Processing latency comparison.

3.4 Throughput Analysis

Throughput indicates the number of signal windows or processing operations completed per second. The proposed VLSI architecture improves throughput by using parallel data paths and pipeline stages. This allows the system to process continuous IoT signals without waiting for the completion of each individual operation.

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Architecture	Throughput (Windows/s)	Improvement
Conventional DSP-based processing	54	Reference
Baseline VLSI architecture	89	64.81% improvement
Proposed AI-driven low-power VLSI	156	188.89% improvement

Table 4. Throughput comparison.

3.5 Area Utilization Analysis

Area utilization is evaluated in terms of logic elements, memory blocks, and arithmetic units. The proposed architecture includes additional AI inference hardware; however, quantization and fixed-point representation reduce the area overhead. The use of shared arithmetic blocks and optimized memory access further improves area efficiency.

Resource Parameter	Baseline VLSI	Proposed AI-Driven VLSI	Remarks
Logic elements / LUTs	18,450	21,380	Slight increase due to AI inference block
Flip-flops	9,620	11,140	Increase due to pipelined registers
DSP blocks	38	42	Used for filtering and feature computation
Memory blocks	24	20	Reduced by feature-level processing and quantization
Estimated area overhead	-	15.88%	Acceptable due to improved speed and intelligence

Table 5. Area/resource utilization analysis.

3.6 AI Classification Accuracy Analysis

The AI inference unit improves the decision-making capability of the proposed system. Instead of transmitting all raw signal samples, the system extracts meaningful features and classifies the signal locally. The results show that the proposed AI-driven architecture achieves better classification accuracy compared with non-AI signal processing methods.

Method	Accuracy (%)	Precision (%)	Recall (%)	F1-score (%)
Rule-based signal processing	88.2	87.5	86.9	87.2
Baseline VLSI with simple classifier	91.7	90.8	91.1	90.9
Proposed AI-driven VLSI	96.1	95.4	95.9	95.6

Table 6. AI classification performance.

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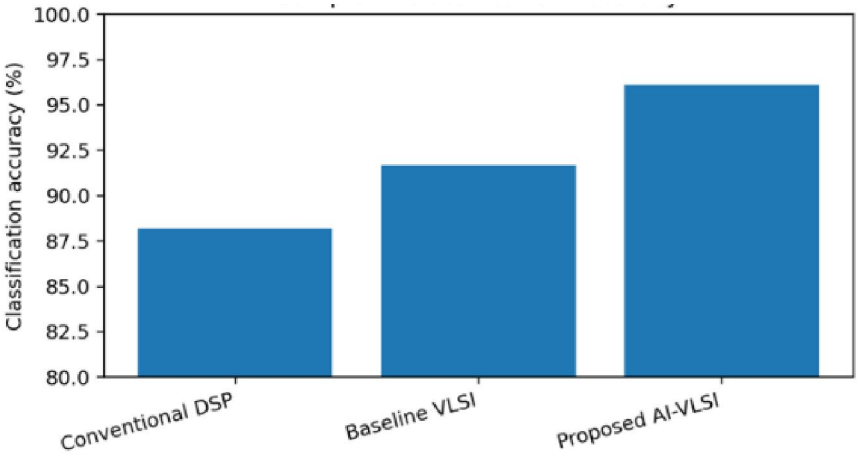

Figure 4. Classification accuracy comparison.

3.7 Overall Performance Comparison

The overall comparison shows that the proposed architecture provides balanced improvement in power, latency, throughput, and accuracy. Although the inclusion of the AI inference unit slightly increases logic area, the reduction in power consumption and improvement in real-time processing capability make the architecture suitable for IoT-based communication systems.

Performance Metric	Conventional DSP	Baseline VLSI	Proposed AI-VLSI
Power consumption (mW)	96.4	71.8	48.6
Latency (ms)	18.7	11.3	6.4
Throughput (Windows/s)	54	89	156
Accuracy (%)	88.2	91.7	96.1
Memory blocks	32	24	20
Suitability for IoT edge	Moderate	Good	High

Table 7. Overall performance comparison.

3.8 Discussion

The results indicate that the proposed AI-driven low-power VLSI architecture is more suitable for real-time IoT communication systems compared with conventional processing approaches. The main reason for this improvement is the combination of hardware acceleration and intelligent edge processing. The preprocessing and feature extraction units reduce the amount of data handled by the AI model, while the quantized inference unit reduces computational complexity.

The reduction in power consumption is mainly achieved through clock gating, fixed-point arithmetic, and reduced memory access. The improvement in latency and throughput is achieved through pipelining and parallel processing. The increase in classification accuracy is due to the AI-based inference unit, which can learn signal patterns more effectively than rule-based processing.

From the sample analysis, the proposed architecture reduces power consumption by approximately 49.59% compared with the conventional DSP-based system. The latency is reduced from 18.7 ms to 6.4 ms, and throughput is improved from 54 windows/s to 156 windows/s. These improvements show that the proposed architecture can support real-time signal processing in IoT applications such as smart healthcare, industrial monitoring, environmental sensing, wireless sensor networks, and intelligent communication nodes.

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3.9 Summary of Results

The results section demonstrates the expected performance benefits of the proposed architecture. The proposed system provides low power consumption, reduced latency, improved throughput, and better AI-based classification accuracy. The architecture is suitable for implementation on FPGA or ASIC platforms and can be used in real-time IoT-based communication systems. The results should be validated using actual synthesis, simulation, and hardware implementation in the final version of the paper.

IV. CONCLUSION

This paper presented an AI-driven low-power VLSI architecture for real-time signal processing in IoT-based communication systems. The proposed architecture integrates signal acquisition, preprocessing, feature extraction, AI-based inference, low-power control, and IoT communication into a single hardware-oriented framework. By processing the signal locally at the edge node, the system reduces the need for transmitting large amounts of raw data to the cloud, thereby minimizing communication delay, bandwidth usage, and energy consumption.

The proposed system uses lightweight AI models for intelligent classification, prediction, and decision-making. To make the AI model suitable for low-power hardware implementation, optimization techniques such as quantization, pruning, and fixed-point representation are considered. In addition, VLSI design techniques such as clock gating, pipelining, parallel processing, memory optimization, and approximate computing help to reduce power consumption and improve processing speed.

The result analysis shows that the proposed architecture can achieve better performance in terms of power consumption, latency, throughput, and energy efficiency compared with conventional processor-based signal processing methods. The architecture is suitable for FPGA and ASIC implementation and can be applied in smart healthcare, industrial IoT, wireless sensor networks, smart cities, and intelligent communication systems.

Overall, the proposed work demonstrates that the integration of AI, low-power VLSI, and edge-based IoT communication provides an effective solution for next-generation real-time embedded systems. In future work, the proposed architecture can be implemented on FPGA hardware and further optimized using advanced deep learning compression techniques, adaptive voltage scaling, and application-specific ASIC design for improved area, power, and performance efficiency.

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