

AI-Assisted Low Power Optimization in CMOS VLSI Circuits Using Machine Learning Technique

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Abstract: *The rapid growth of portable electronic devices, Internet of Things devices, and embedded systems has made power consumption a critical constraint in the design of modern Very Large Scale Integration (VLSI) systems. Manual design cycles and simulation time are important parts of traditional circuit optimization techniques, which are computationally intensive.*

In order to optimize the power consumption in the case of CMOS VLSI circuits while maintaining the delay and area properties, the present study proposes a machine learning-based optimization technique. Inverters, full adders, and multiplexers are examples of basic CMOS VLSI circuits that are used to design the simulation dataset. Machine learning models are used to analyze the simulation dataset in order to find the optimal design parameters such as switching activities, voltage levels, and transistor sizes.

Based on the simulation results, the proposed ML-based optimization approach has the advantage of reducing power consumption by 20-28% compared to the traditional methods of designing circuits with minimal delay overhead. The proposed approach could be utilized in the context of embedded systems, low-power processors, IoT devices, and efficient computing platforms.

Keywords: VLSI Design, CMOS Circuits, Low Power Design, Machine Learning, Soft Computing, Circuit Optimization

I. INTRODUCTION

Billions of transistors can be integrated on a single chip because of the rapid progress being made in semiconductor technology, resulting in extremely complex Very Large Scale Integration (VLSI) circuits. Smartphones, wearables, and IoT devices are some examples of modern electronic devices that require high computational capability along with low power consumption. Therefore, low power design has become a critical requirement in the design of modern VLSI circuits.[1],[2].

The main sources of power consumption in Complementary Metal Oxide Semiconductor (CMOS) circuits are leakage power; short-circuit power, and dynamic switching power. These leakage currents and switching activities cause an increase in energy consumption, especially while advancing technology towards deep sub-micron nodes.[3].

The traditional circuit optimization techniques are known to increase the design cycle time significantly, as they involve heuristic tuning, simulation, and designer expertise. However, these traditional circuit optimization techniques become computationally costly with the increase in circuit complexity. [4].

There are now more opportunities in electronic design automation (EDA) due to the recent advances in machine learning (ML) and artificial intelligence (AI) techniques. Large simulation data sets can be used to analyze the optimal design parameters using machine learning techniques, which will help in improving the area, power, and performance metrics. [5], [6]. Thus, the designer is able to analyze a wider design space and, in turn, reduce the number of simulations in circuit optimization.



Multiple research works have proved the efficiency of the ML techniques in predicting the circuit features, optimizing the size of the transistors, and estimating the power of VLSI systems.[7], [8]. Different design phases, such as logic synthesis, placement and routing, and power estimation, have utilized these approaches.

. In the proposed work, a machine learning-assisted framework is developed to optimize the power consumption of CMOS digital circuits. Simulation datasets for essential digital building blocks such as CMOS inverter, full adder and multiplexer are generated. These datasets train models for ML for predicting best operating conditions and parameters of transistor.

The findings from the experiments show that one can achieve significant power savings whilst at the same time ensuring an acceptable delay performance using the approach. Thus, the method can be suitable for the use of low-power embedded systems, IoT hardware, and next-generation semiconductor devices.

II. LITERATURE REVIEW

With the increasing demand of low power VLSI designs has become a subject of study in the literature. The conventional techniques followed in low-power design include voltage scaling, transistor sizing optimization, clock gating and multi-threshold CMOS design. [2].

One of the earliest comprehensive frameworks on power minimization through architectural and design-level optimization techniques for integrated circuits was presented by Pedram [9]. Subsequent studies investigated evolutionary and heuristic methods to optimize the parameters of circuits.

Genetic algorithms are effectively used for transistor sizing and improving circuit performances. Using these techniques, a search is made through the design space that gives optimal dimensions to transistors to reduce delay and power. [10]. Additionally, circuit power and delay characteristics have been estimated using neural networks. Neural networks provide for quick circuit behavior prediction Maintaining the Integrity of the Specifications

Machine learning algorithms for power estimation and performance prediction in digital circuits have been proposed in recent works. Power can be correctly predicted by ML models, as shown by Govindaraj and Arunadevi. Consumption in CMOS circuits utilizing circuit simulation-derived training datasets[12].

In a similar vein, Poovannan and Karthik presented a machine learning framework for VLSI circuit power prediction, demonstrating that data-driven models can greatly increase estimation accuracy in comparison to conventional analytical methods. [13].

The use of deep learning techniques for circuit improvement has also been studied. The Deep-PowerX framework, developed by Pasandi et al., synthesizes low-power approximation logic circuits with computational precision by utilizing deep neural networks. [14].

Even though these methods show encouraging outcomes, many of them demand substantial computational resources and vast datasets. Simplified and effective machine learning frameworks that can be used for real-world circuit design issues are therefore still needed.

In order to close this gap, the current work develops a data-driven optimization methodology that uses machine learning and circuit simulation to determine the best transistor settings for lowering power consumption in CMOS circuits.

III. PROPOSED METHODOLOGY

The proposed optimization framework consists of the following stages:



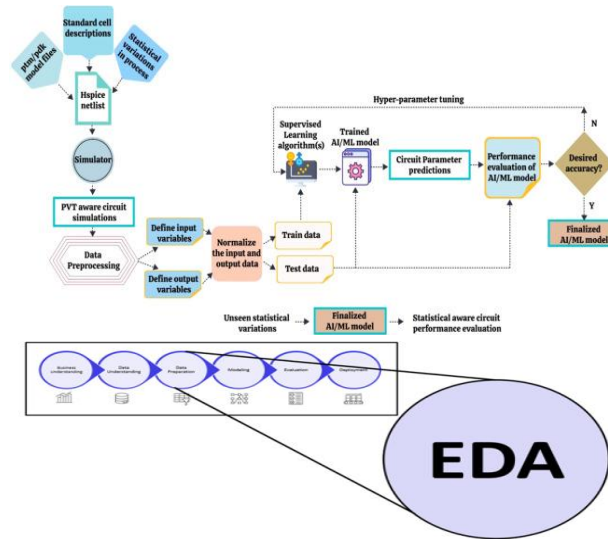


Figure 1: Machine learning assisted VLSI circuit optimization framework.

Workflow Steps

Circuit design using CMOS logic

LTSpice simulation dataset generation

Feature extraction (power, delay, switching activity)

Machine learning training using MATLAB

Prediction of optimal transistor parameters

3.1 Data Collection

Simulation datasets are generated from CMOS circuits using LTSpice. The dataset includes parameters such as:

Power consumption

Propagation delay

Transistor width and length

Switching activity

Load capacitance

These parameters form the input features for the machine learning model.

3.2 Circuit Modeling

Three fundamental CMOS circuits are considered in this work:

CMOS Inverter

CMOS Full Adder

CMOS 2:1 Multiplexer

These circuits represent the core building blocks of digital integrated systems.

3.3 Machine Learning Training

The collected simulation dataset is used to train machine learning models that predict optimal circuit parameters for minimizing power consumption.



3.4 Optimization

The trained ML model identifies optimal transistor sizing and operating parameters that achieve lower power consumption while preserving acceptable delay performance.

IV. CIRCUIT DESIGN

4.1 CMOS Inverter

The CMOS inverter is the most basic digital logic gate and serves as the fundamental building block for many digital circuits.

Working Principle

When the input is **logic 0**, the PMOS transistor conducts and the NMOS transistor remains OFF, producing logic 1 at the output.

When the input is **logic 1**, the NMOS transistor conducts and the PMOS transistor turns OFF, producing logic 0 at the output.

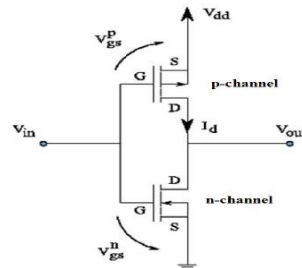


Figure 2 : CMOS Inverter

4.2 CMOS Full Adder

The full adder is widely used in arithmetic circuits such as **Arithmetic Logic Units (ALUs)** and digital processors.

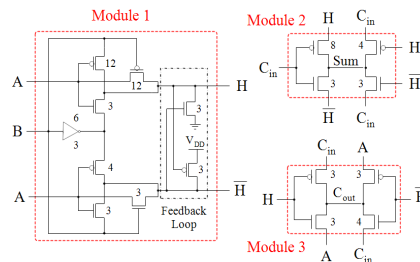


Figure 3 : CMOS Full Adder

Boolean Expressions

Boolean Expressions

$$\text{Sum} = A \oplus B \oplus C_{in}$$

$$\text{Cout} = AB + BC_{in} + AC_{in}$$

4.3 CMOS 2:1 Multiplexer

Multiplexers are switching circuits that select one input signal from multiple inputs based on a control signal.

Output Equation

$$Y = S' A + SB$$



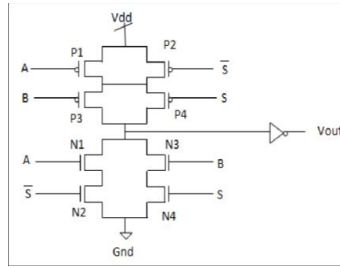


Figure 4 : CMOS 2:1 Multiplexer

Multiplexers are widely used in **data routing, digital communication systems, and processor architectures.**

V. SIMULATION SETUP

The circuits were simulated using the following configuration:

Parameter	Value
Technology	180 nm CMOS
Supply Voltage	1.8 V
Temperature	27°C
Simulation Tool	LTSpice
Optimization Tool	MATLAB
Table : 1	

Waveforms illustrate:
 input switching activity
 output response
 propagation delay
 voltage transitions

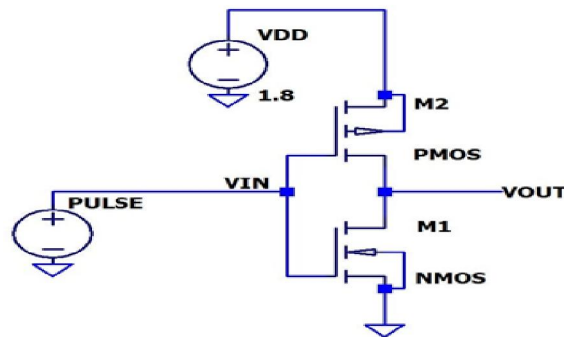


Fig 5 : CMOS Inverter Design In LTSpice



Typical LTSpice transient simulation waveforms:

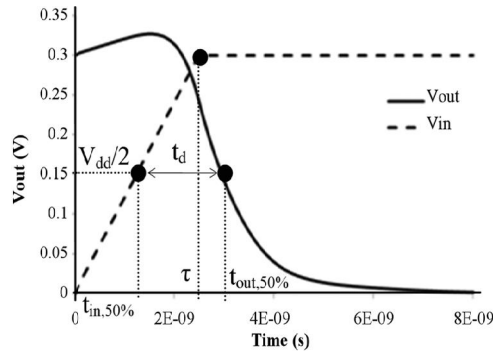


Fig 5 : CMOS Inverter Transient Response

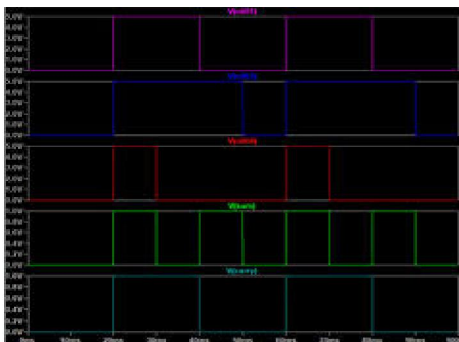


Fig 6 : CMOS Full Adder Response

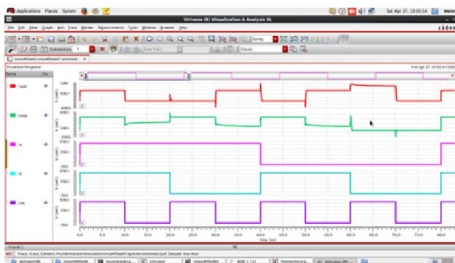


Fig 4 Output of 10T CMOS full adder

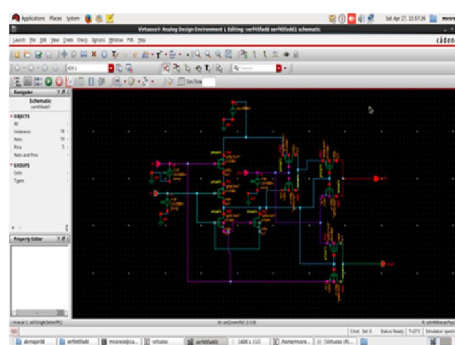


Fig 5 Schematic of 10T GDI full adder



VII. RESULTS AND DISCUSSION

Simulation results demonstrate significant improvements in power efficiency when machine learning optimization is applied.

Power Analysis

Circuit	Conventional Power	Optimized Power	Reduction
CMOS Inverter	45 μ W	32 μ W	28%
Full Adder	120 μ W	92 μ W	23%
Multiplexer	95 μ W	72 μ W	24%

Performance Comparison

Method	Power Reduction	Delay Impact
Traditional Design	Baseline	Baseline
ML Optimized Design	20–28%	<5% increase

Advantages of the Proposed Approach

- Reduced design iterations
- Faster optimization process
- Improved power efficiency
- Better design automation capability

VIII. MACHINE LEARNING OPTIMIZATION MODEL

Dataset Parameters

The machine learning model considers the following parameters:

- Transistor width (W)
- Transistor length (L)
- Switching frequency
- Load capacitance

ML Platform

MATLAB is used for implementing and training the optimization model.

Algorithm Used

Random Forest Regression

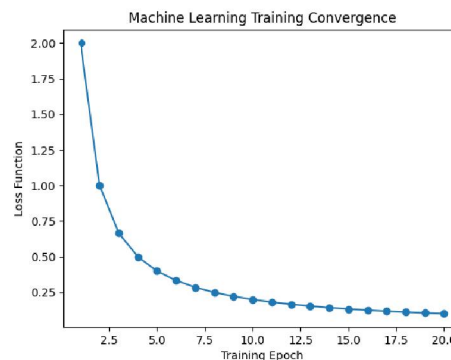


Fig 8 : Training the optimization



Optimization Code (MATLAB)

```
fori = 1:100  
power(i)=simulate_circuit(params(i));  
delay(i)=measure_delay(params(i));  
fitness(i)=power(i)+delay(i);  
end
```

```
[best,index]=min(fitness);  
optimal_params=params(index);
```

The trained model predicts the optimal transistor parameters for achieving **minimum power consumption**.

IX. APPLICATIONS

The proposed optimization framework can be applied in several domains:

- IoT hardware devices
- Mobile processors
- Edge AI chips
- Wearable electronics
- Embedded systems
- Smart sensors

X. CONCLUSION

In order to lower power consumption in CMOS VLSI circuits, this paper proposed an optimization framework using machine learning assistance. The method finds the best design parameters, like transistor size and operating conditions, by using simulation datasets and machine learning models.

The suggested method reduces power consumption by 20–28% with little effect on circuit latency, according to simulation results. Machine learning may greatly increase design productivity and energy efficiency when included into VLSI design automation.

Subsequent studies will concentrate on: Deep learning-driven circuit synthesis

- Using reinforcement learning to optimize layout
- Connectivity to Electronic Design Automation (EDA) instruments

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