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Leakage Power Reduction in Low-Process-Technology VLSI Circuits Using Regulated Cross-Coupled and Split Inverter Techniques

D Nitya Santoshi Rupa[1] and M Veeresh Kumar[2]
Assistant Professor, Department of Electronics and Communication Engineering[1,2]
Annamacharya Institute of Technology and Science's, Hyderabad, Telangana, India

Abstract: *This work presents a novel power-efficient level shifter design that integrates a regulated cross-coupled (RCC) network with a SAPON-based split inverter to achieve significant reductions in both leakage and dynamic short-circuit power. The RCC network effectively minimizes power loss in the pull-up path, while the split inverter at the output ensures reduced short-circuit current during switching transitions. To further enhance performance, a modified split inverter with an added load capacitor is employed, which accelerates switching speed, stabilizes node voltages, and improves overall energy efficiency. The proposed design operates reliably in the sub-threshold region, accommodating voltage levels from 0 V to 0.5 V for 50 nm technology and 0 V to 0.9 V for 90 nm technology, while achieving nearly 31–32% power savings compared to conventional level shifter designs. Comprehensive LTspice simulations validate the functionality, demonstrating low leakage currents, high-speed transitions, and stable operation across multiple input cycles, indicating its suitability for modern low-power VLSI systems and multi-voltage domain applications.*

Keywords: Level shifter, split inverter, regulated cross-coupled network, threshold voltage, leakage reduction, short-circuit power.

I. INTRODUCTION

A level shifter is a circuit used to convert signals from one logic voltage domain to another, making it essential in interfacing circuits such as CMOS and TTL. They are widely applied in processor design, sensor interfaces, and VLSI systems, where operating voltages such as 3.3 V, 1.8 V, or even lower are commonly required. In digital systems, level shifters enable different blocks to operate at distinct voltage levels, which would otherwise be difficult to achieve. While down-conversion (high-to-low) is sometimes optional, up-conversion (low-to-high) is almost always necessary. Depending on the application, level shifters can be placed at the top, bottom, or even within intermediate stages of a circuit.

Power dissipation in digital systems primarily depends on supply voltage, load capacitance, operating frequency, and switching activity. Lowering these factors can significantly reduce power consumption; for example, halving the supply voltage reduces dynamic power by nearly 75%, although at the cost of performance degradation. In CMOS transistors, both static and dynamic power are present: leakage power occurs in the OFF state, while short-circuit and switching power dominate dynamic power during circuit activity. Several techniques such as transistor sizing, clock gating, power gating, logic optimization, multiple supply voltages, pipelining, and parallel processing are commonly employed to reduce dynamic power. However, reducing supply voltage is the most effective approach, even though it negatively impacts speed. To address this tradeoff, applying different supply voltages to different functional blocks using level shifters offers a practical solution. Furthermore, level shifters based on a cross-coupled network not only minimize power dissipation but also improve output speed, making them suitable for a wide range of input voltage levels.

In digital systems, the primary design challenges are area, delay, and power dissipation. Among these, excessive power dissipation is a critical concern, as it shortens battery lifetime and increases the need for cooling mechanisms. Power

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consumption can be minimized by lowering the switching activity factor, reducing load capacitance, scaling down supply voltage and operating frequency, and optimizing device dimensions (W/L ratio).

Power dissipation in CMOS circuits can be broadly classified into static power and dynamic power.

Static power is present when the circuit is idle and mainly arises from leakage currents. The key sources of leakage include:

- Sub-threshold leakage current occurs when a transistor is in the off state but still allows a small current to flow between source and drain. This happens because even when the gate-to-source voltage is below the threshold, weak inversion allows carriers to move through the channel. It increases static power consumption, especially in scaled technologies.
- Drain-induced barrier lowering (DIBL) takes place when a high drain voltage reduces the threshold voltage of the MOSFET. The drain potential lowers the energy barrier in the channel, making it easier for carriers to pass even at low gate voltages. This increases leakage and weakens gate control.
- The punch-through effect happens when the depletion regions from the source and drain extend into the channel and overlap. This provides a direct path for current between source and drain, bypassing gate control. It usually occurs in very short-channel devices.
- Gate-induced leakage is caused by tunneling of carriers through the thin gate oxide layer. As oxide thickness decreases in advanced technologies, strong electric fields allow electrons or holes to tunnel, adding to overall leakage current.
- Short-channel effects appear when the channel length becomes very small compared to the depletion regions. In this case, the gate's control over the channel weakens, leading to threshold voltage roll-off, increased leakage, and enhanced effects like DIBL and punch-through.
- Reverse-bias junction leakage occurs at the source-body and drain-body junctions, which are reverse-biased during operation. Minority carriers in the depletion region generate current across these junctions. Although small, it becomes more significant in scaled devices.

Together, these effects highlight the challenges of transistor scaling in deep submicron technologies, where effective leakage control and device design are critical for achieving low-power VLSI systems.

Dynamic power occurs during switching activity and is dominated by switching power and short-circuit power. Short-circuit power appears when both NMOS and PMOS transistors conduct simultaneously due to mismatched rise and fall times of input transitions.

Leakage power, although initially a minor contributor, becomes increasingly dominant as technology scales down and channel lengths shrin as shown in **Fig.1.** Notably, leakage is present not only in static mode but also during active operation, where it can exceed the dynamic power at deep-submicron technology nodes. Thus, effective control of leakage and dynamic power is essential for achieving low-power VLSI designs as shown in **Fig.2.**

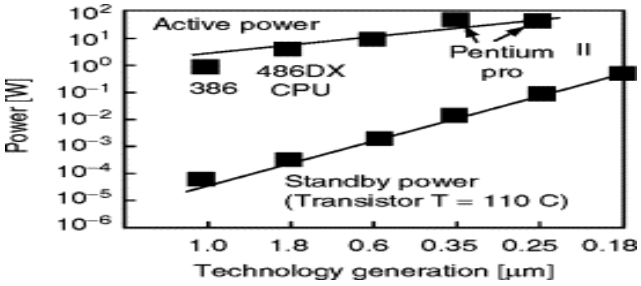

Figure.1: Power Vs Channel length

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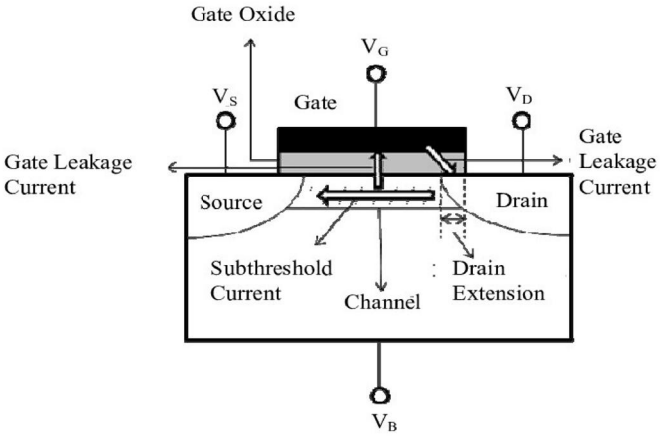

Figure.2: Leakage currents

In dynamic power dissipation, the dominant components are switching power and short-circuit power, where short-circuit power occurs between the supply voltage and ground when both transistors conduct simultaneously due to mismatched rise and fall times of input transitions; leakage power, on the other hand, is present in MOS devices during both static and dynamic operation, and in fact increases significantly as technology scales down, eventually becoming the dominant contributor when channel length is reduced; overall, major sources of power dissipation include switching power, which depends on activity factor, load capacitance, supply voltage, and operating frequency, static leakage power, which arises mainly from reverse-biased junctions and sub-threshold current influenced by thermal voltage and threshold voltage, and short-circuit power, which results from transient conduction of NMOS and PMOS during input signal transitions.

1. Switching power

It occurs when output is switching from one state to another it depends on

activity factor
decreasing load capacitance
decreasing voltage
step-down frequency

$$P = \alpha * f * C * Vdd^2$$

2. Static leakage power

In CMOS circuits, static leakage power is the power consumed when the circuit is not switching. It mainly comes from two sources: reverse-biased P–N junction leakage at the source and drain regions, and sub-threshold leakage current when the gate voltage is below the threshold but a small current still flows. This leakage can be observed by biasing the transistor in the OFF condition. For an NMOS, the gate is tied to ground while the drain is connected to the supply. Under these conditions, any small current that flows from drain to source is leakage. For a PMOS, the same can be done by setting the gate to the supply voltage while the source is grounded.

By running an operating point simulation, LTspice directly reports this leakage current. Multiplying this leakage by the supply voltage gives the static leakage power. For example, in 90 nm technology, the leakage is noticeably smaller compared to 50 nm, which makes the overall static power lower.

To study sub-threshold behavior, a DC sweep of the gate voltage can be performed. In the sweep, the drain is kept at the supply voltage and the gate voltage is gradually increased from 0 V up to above the threshold. The resulting current curve shows the weak inversion region, where the current increases rapidly with gate voltage even before the transistor

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is fully ON. This helps identify how strongly leakage depends on the difference between the gate voltage and the threshold voltage.

3. Short leakage power

Short-circuit leakage power occurs during input transitions when both NMOS and PMOS transistors conduct simultaneously for a short period, creating a direct current path from the supply to ground, often caused by mismatched rise and fall times of the input signal.

An inverter is a basic circuit in which the output is always the complement of the input. When the input is logic '0', the PMOS transistor conducts while the NMOS transistor is turned off, allowing the supply voltage to charge the output capacitor and produce a logic '1' at the output. Conversely, when the input is logic '1', the NMOS transistor conducts and the PMOS transistor is turned off, causing the output capacitor to discharge to ground and generate a logic '0'. To minimize leakage power in this design, two additional transistors (Q1 and Q2) are introduced, with the gate of each connected to the source of the other. This configuration forms an effective stacking structure between the supply voltage and ground, thereby lowering power consumption. During each input transition, one of the added transistors remains in the cut-off region, providing high resistance and significantly reducing leakage power dissipation.

Several studies have focused on reducing leakage and short-circuit power in VLSI circuits through innovative level shifter and low-power design techniques. Usami et al. [1] proposed using multiple supply voltages to minimize leakage in media processors, while Alioto [2] provided a comprehensive tutorial on ultra-low power VLSI design, covering both theoretical and practical approaches. Maghsoudloo et al. [3] and Hosseini et al. [4] developed high-speed, ultra-low power sub-threshold and dual-supply voltage level shifters, respectively, emphasizing energy-efficient voltage conversion. Luo et al. [5] improved level shifter efficiency using a modified Wilson current mirror hybrid buffer, whereas Wen et al. [6] introduced a self-controlled current limiter to reduce leakage while maintaining performance. Lanuzza et al. [7,8] presented ultra-low voltage and multi-supply voltage level shifters for enhanced energy efficiency, and Huang and Chiou [9] proposed a limited contention cross-coupled level shifter for efficient sub-threshold to super-threshold conversion. Techniques such as LCNT [10], input control [11], and LECTOR [12] have been used to minimize leakage in CMOS circuits, complemented by sleep-state approaches [13] and practical leakage reduction strategies [14]. Recent surveys [15,16] summarize modern methods for leakage power reduction in low-process technology VLSI circuits, highlighting the ongoing trend of combining circuit-level innovations with sub-threshold operation to achieve high-speed, energy-efficient designs.

II. MPLEMENTATION OF LS WITH SAPON SPLIT INVERTER

LS with split inverter is used at the output and this split inverter is implemented with SAPON technique is used to reduce both leakage power and short-circuit power. During input transition from 1to0, N1 node is at HIGH and value N2 node is at low, it will switch on T2, T3 and T1, T4 will be OFF. When input transition 0 to 1 T7 will be ON and T8 will be OFF. It will pull the value N1 to low and when it is discharging, T1, T4 will switch ON and T2, T3 are switched OFF. At this instant, the N2 node will start charging, as the output is connected to N2 through the capacitor.

The capacitor will charge to the value of N2. Here PMOS transistors will go to the sub-threshold region but will never be switched off because the get input value of V_{DDH}-V_{th}. Pull up transistors will never go to switched-OFF, causes to speed of response is increased. When input transition at input, the same process is repeated but in inverse N1 node to be HIGH and N1 node will be at LOW.

III. SIMULATION RESULTS

Fig. 3 and **4** illustrate the schematic and simulation results of the proposed level shifter (LS) with a regulated cross-coupled (RCC) network and SAPON inverter implemented in 50 nm and 90 nm technologies, respectively. In the 50 nm technology implementation (**Figure 3**), the input pulse is applied with rise and fall times set to zero, an initial voltage of 0 V, and a threshold (Von) of 0.25 V. The pulse is defined with a Ton of 10 ms, a time period of 20 ms, and 5 cycles. The PMOS transistors (M1, M2, M3, M4, M5, M6, M10, M12, M13) are sized with a width-to-length (W/L) ratio of 0.4 µm/50 nm, while the NMOS transistors (M7, M8, M9, M11, M14) use a W/L ratio of 0.2 µm/50 nm. Under

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these conditions, the circuit operates in the sub-threshold region from 0 V to 0.5 V. The measured power dissipation is 88 nW, and the leakage current is 246 µA.

In the 90 nm technology implementation (**Figure 4**), the input pulse is also applied with rise and fall times of zero and an initial voltage of 0 V, but the threshold voltage Von is set to 0.45 V. The pulse parameters are defined with a Ton of 10 ms, a time period of 40 ms, and 30 cycles. The transistor sizing is similar, with the PMOS devices using a W/L ratio of 0.4 µm/90 nm and the NMOS devices using a W/L ratio of 0.2 µm/90 nm. In this case, the circuit operates in the sub-threshold region from 0 V to 0.9 V. The design shows improved performance compared to the 50 nm version, with a reduced power dissipation of 72 nW and a leakage current of 129 µA.

From this comparison, it is observed that both designs achieve reliable sub-threshold operation. However, the 90 nm implementation demonstrates better efficiency, as it not only supports a wider sub-threshold voltage range but also achieves lower power dissipation and reduced leakage current compared to the 50 nm implementation. This makes the 90 nm design more suitable for ultra-low power VLSI applications.

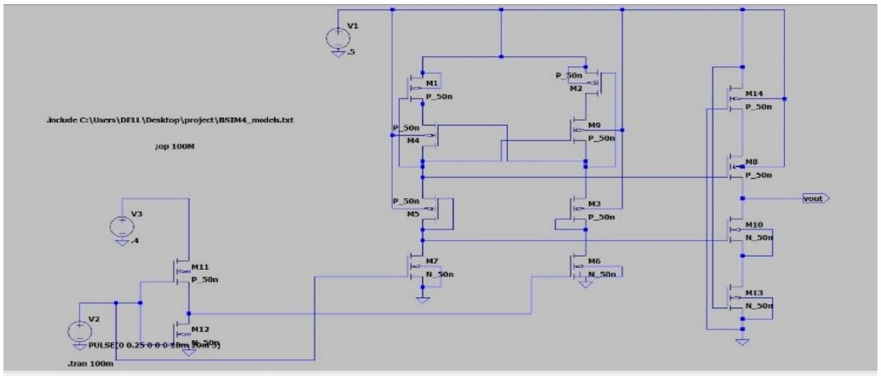

Figure 3. 50 nm technology based Schematic Diagram of LS using SAPON Inverter

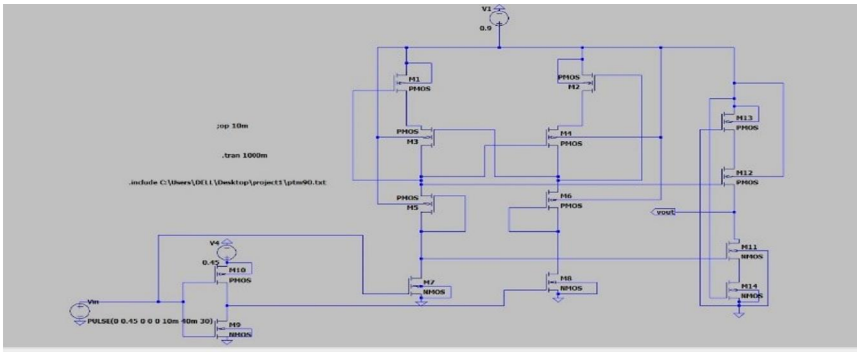

Figure 4. 90 nm technology based Schematic Diagram of LS using SAPON Inverter

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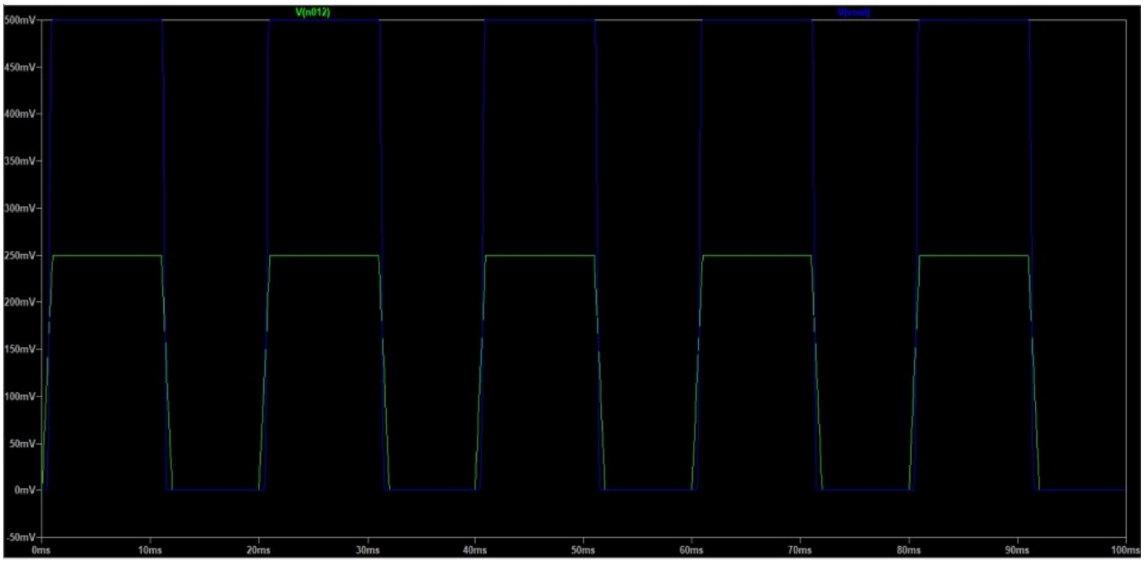

Figure 5. Simulation Results of 50nm Technology

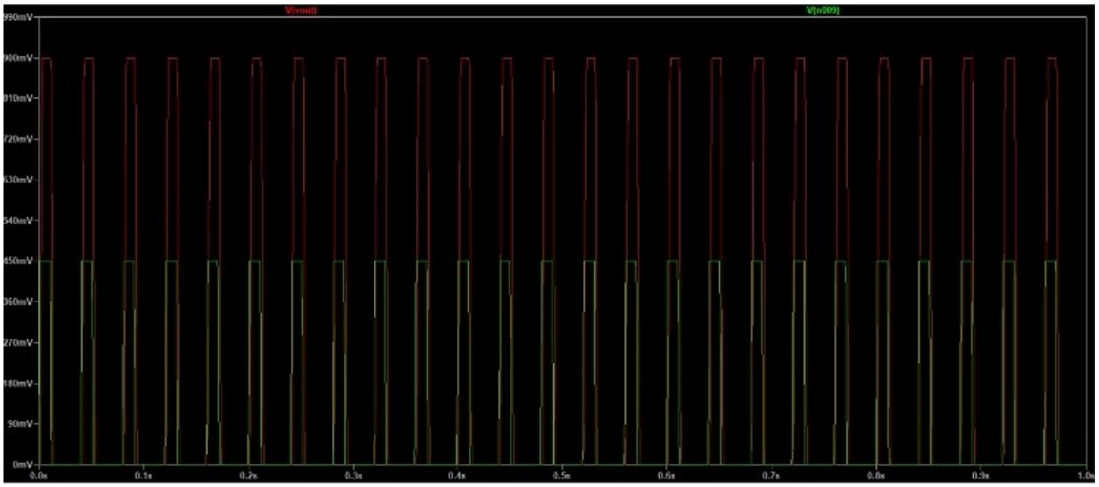

Figure 6. Simulation results of 90nm Technology

IV. CONCLUSION

The proposed level shifter demonstrates a highly efficient approach to reducing both static leakage and dynamic short-circuit power by combining a regulated cross-coupled network with a SAPON-based split inverter. The design ensures fast and reliable switching, as the PMOS transistors operate in the sub-threshold region without being fully turned off, maintaining conduction and improving response speed. Simulation results in 50 nm and 90 nm technologies show power dissipation as low as 88 nW and 72 nW, with corresponding leakage currents of 246 µA and 129 µA, respectively, confirming significant energy savings. By operating effectively at sub-threshold voltages and achieving approximately 32% reduction in leakage power, this level shifter is particularly suited for low-power, high-performance VLSI circuits, multi-supply voltage designs, and applications where minimizing energy consumption is critical, such as portable and battery-powered devices. The proposed architecture also highlights the practical integration of RCC and SAPON techniques to simultaneously optimize speed, power, and reliability, making it a promising candidate for next-generation low-power digital systems.

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AUTHORS PROFILE

D. Nitya Santhoshi Rupa received her B.Tech degree from Methodist Institute of Engineering Tecchnology,Affiliated to OU, Hyderabad, and completed her M.Tech in VLSI System Design from Holy Mary Institute of Science and Technology, JNTUH, Hyderabad. She is currently working as an Assistant Professor at Annamacharya Institute of Technology and Sciences, Hyderabad. Her areas of interest include VLSI and image processing.

M. Veeresh Kumar received the B.Tech degree from Kottam Tulasi Reddy Memorial College of Engineering in 2011 and completed M.Tech in VLSI System Design from Sri Chaitanya College of Engineering and Technology in 2014. He is currently working as an Assistant Professor at Annamacharya Institute of Technology and Sciences, Areas of interest include VLSI & Signal processing and image processing