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Systems used for Power-Constrained Testing of Digital Circuits: A Review of DFT and Power Management Integration

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Abstract: *The low power consumption is a critical demand in the design and testing of the modern VLSI architecture and a System on a Chip (SoC). Under a test mode, untamed switching activities can make the power requirements of the device far higher than that of being functional thereby creating a lot of thermal stress and even damaging the circuit and making tests expensive in the process. Several power-conscious test methods have been developed to counter these issues and they target low switching activity testing and regulation of peak power without sacrificing fault coverage. They encompass state-of-the-art test vector optimization including: vector reordering, compression, and X-plus scan chain reordering and clock gating plans. Energy efficiency is further increased with low-power Built-In Self-Test (BIST) design and with adaptive testing whose accuracy depends on monitoring of real-time power. Scalable and power-efficient tests with large and complex systems are possible through hierarchical and modular design Design-for-Test (DFT) methodologies. Real-time power adaptation can be done through techniques such as Dynamic Voltage and Frequency Scaling (DVFS) and AI-based algorithms and metaheuristic methods can be used to plan tests and optimize testing. This review expounds on such options in detail, with synthesis and power management as a major enabling factor in robust, scalable, and energy-efficient testing in next-generation digital systems.*

Keywords: Power-constrained testing, Lower-Power VLSI circuits, System-on-Chip (SoC) Testing, Design-for-Test (DFT), Built-In Self-Test (BIST), Test power management

I. INTRODUCTION

Power consumption dissipated during testing, often labeled test power, is a critical concern in the development and testing of very large scale integration (VLSI) circuits, whether they are low-power or high-performance[1]. Complex System-on-Chip (SoC) designs are particularly prone to power consumption spikes during test mode compared to normal functioning operation. [2]. This elevated test power can result in thermal issues, circuit degradation, timing failures, or even permanent device damage, ultimately impacting product quality and increasing overall testing costs. Consequently, low-power testing techniques have become essential for the successful implementation and mass production of energy-efficient digital systems.

One of the major contributors to excessive test power is the high switching activity caused by the low correlation between successive test vectors. This increased activity leads to a surge in dynamic power dissipation during scan testing[3]. Although techniques such as test vector reordering, compaction, and X-filling have been proposed to increase vector correlation and reduce transitions, they often come with the trade-off of increased test application time posing another challenge in balancing power, performance, and test efficiency.

The exponential expansion in transistor density and integration levels can be attributed to Moore's Law, which has propelled the exponential growth of circuit complexity[4]. This complexity introduces multiple design trade-offs across power, area, speed, test data volume, and test energy. To overcome these problems, the industry is making greater use of Design-for-Test (DFT) methodologies that are power and performance-conscious[5]. The process of assessing such architectures is usually performed with tools such as Xilinx soft cores, which present the hardware characteristics that

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are suitable to low-power scaled-up testing.

In addition, the growth in semiconductor technologies has compounded manufacturing tests mainly in the area of large-scale designs of VLSI[6]. The absence of correlation between vectors not only escalates switching activity, but also leads to high power levels of dissipation and inefficient test[7]. Here BIST seems to provide a very viable solution especially when the idea has been integrated with power-sensitive applications like in the use of test vectors duties facilitated by use of Linear Feedback Shift registers (LFSRs) and low-transition pattern generators.

In order to be most effective in the power dissipation reduction, the techniques require application at many levels of abstraction, including device and circuit levels, architectural, and algorithmic levels. Power is also affected at the device level due to aspects like threshold voltage (Vth), transistor sizing and interconnect modelling [8]. The choice of design style, clock gating design and minimization of the voltage swings are important at the circuit level. In the meantime, architectural level optimizations comprise of pipelining, parallelism, excellent bus design, and dynamic management of power among the system blocks.

This overview discusses a set of methods that is rather extensive when it comes to the power-constrained testing, with a closer emphasis on the synergy between DFT and power management techniques. It shall offer an insight regarding the current work, problems and needs over the future scope of energy efficient and dependable testing in the present digital sophisticated systems.

A. Structure of the paper

The paper is structured in the following way: Section II presents the basic principles of Design-for-Testability (DFT), especially focused on the power-constrained methods of test. Section III is about low-power DFT architectures and practical implementation. Section IV discusses the integration of power management strategies with testing processes to enhance energy efficiency. In Section V, offer a comprehensive literature analysis of current research in the subject. Section VI provides a brief summary of the paper's main points and a roadmap for further study into low-power testing in contemporary digital systems.

II. POWER-CONSTRAINED TESTING TECHNIQUES

Power-constrained testing techniques for low-power VLSI and SoC designs focus on minimizing switching activity and scheduling test operations under strict power caps [9]. Common strategies include test vector reordering such as Hamming-distance or AI-based ordering to reduce toggling during scan capture X-filling and do-not-care bit filling heuristics (e.g. genetic-algorithm or probability based) to lower capture power while preserving fault coverage and low-power BIST/LFSR pattern generation schemes that insert intermediate patterns or tune signal probabilities to suppress transitions during shift and capture cycles System-level methods involve power-aware test scheduling, especially in multi-core and 3D integrated circuits, using wrapper/TAM co-optimization and bin-packing or scheduling models that cap test power to safe levels while minimizing total test time[10]. A more modern method sequences test vectors in complicated cores and 3D ICs using metaheuristics like particle swarm optimisation and genetic algorithms to minimise toggling while balancing fault coverage.

A. Test Vector Optimisation

Test vector optimisation is a key technique in power-constrained testing aimed at reducing switching activity and ultimate power consumption during the application of test patterns. In digital circuits, especially during scan-based testing, unoptimized test vectors can lead to excessive transitions between logic states, resulting in increased power dissipation. To overcome this, several test vector optimisation techniques have been devised among them, vector reordering, vector compaction and test data compression[11]. The sequence of test vectors reordered by vector reordering is adjusted so that consecutive patterns become easier to correlate resulting in a reduction of transition density [12]. Compaction of vectors is used to downsize the size of test vectors required without jeopardizing fault coverage which reduces power consumption and test time. Compressing test data also reduces the amount of data transferred and stored, which in turn reduces the amount of energy needed to run the test.

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B. Test Sequence Reordering

The proposed technique of re-ordering the test sequence has the objective of generating consistent power profiles such that simple power approximation models of power can capture the dissipation truthfully [13]. The new power approximation model's power profile was optimized by reducing real power and rearranging the test sequence. As input, they have the transition graph (TG), where each node represents a vector in the test sequence. This power that is lost in the transition between the terminal node vectors is labeled on every edge. The edges that have low weight are then put at the beginning portion of a Hamiltonian path in TG and the edges having higher weight are stored at the end of the path. Power dissipation is determined by multiplying the average power dissipation per transition, per library cell connected to a node in the netlist by the transition count. Figure 1 shows the PPs of the c432 circuit as they appear in the ISCAS85 benchmark set. The nonstandard PP is characterized by a starting low activity area and an ending high activity area, which can be explained by the mentioned reordering strategy to tests.

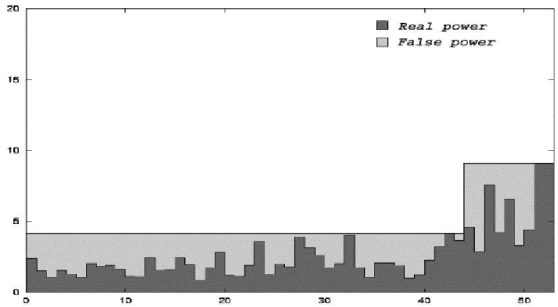

Fig. 1. Power Profiles (PP) for Benchmark Circuit C432

C. Clock Gating and Scan Chain Techniques

The combinational component of the control block is a mapping circuit with m inputs and n outputs, where m is the number of control bits and n is the number of scan chains. In order to produce each output, this XOR network XORs a specific subset of the control bits. The XOR logic architecture guarantees high encoding efficiency, attaining an almost 100% success rate in encoding the designated gating signals in relation to the available control bits. The control circuitry operates [14], for scan chains with designated bits, the appropriate gating signals are chosen to ensure that the input to their respective AND gates is configured to logic '1'. This enables the decompressor to directly drive these scan chains. This task persists until the established power consumption thresholds are achieved. The remaining scan chains that could not be explicitly encoded can have their gating signals determined using the XOR network and the defined control bits. The decompressor is able to actively regulate around half of these scan chains thanks to the gating circuitry shown in Figure 3, with the remaining ones statically maintained at logic '0'.

III. LOW-POWER DFT ARCHITECTURES

A Discrete Fourier Transform (DFT)-based architecture is proposed to address power and hardware efficiency challenges, offering a competitive alternative to the Fast Fourier Transform (FFT). Compared to FFT, the DFT requires fewer iteration cycles, leading to lower hardware utilization and reduced power consumption. The architecture is both a low-power and high-speed architecture and implemented using Altera Quartus design suite [15]. It is implemented as a portable format Verilog-HDL that is built using Synchronous Dataflow Graph (SDFG) specification to facilitate efficient and scalable synthesis [16]. The important features of the proposed architecture are:

- Low power consumption: Optimised for minimal switching activity and efficient resource utilisation, reducing overall power usage during operation.
- Scalable for Any Transform Size: Easily adaptable to different DFT sizes without significant changes in the architecture or performance overhead.
- Low Initial Latency: Capable of delivering faster initial output, making it suitable for real-time and high-speed applications.

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- Reduced Hardware Cost: Utilises fewer logic elements and simpler control logic, lowering implementation costs in hardware.
- Low Computational Complexity: Designed with an efficient dataflow and structure, ensuring minimal algorithmic and architectural complexity.

A. Existing Scan Logic and ATPG Methods

A new wave of scan-based BIST patterns that efficiently cover faults while consuming very few resources in their execution. The suggested BIST reduces switching activity during BIST by reducing the number of transitions at scan inputs during scan shift operations[17]. The suggested BIST consists of two types of TPGs: LT-RTPG and 3-weight WRBIST TPG, implemented scan logic on RTL design, speed analysis, difficulties and remedies for 56 Gbps as well as 112 Gbps PAM4 SerDes. Consequently, developing DFT for greater performance in terms of speed edge of an appliance familiarizes the age-old difficult of performance degradation due to the addition of extra circuitry. Capture-per-clock hybrid assay detail in which the logic of BIST was discussed. Here, a description of the composite examine point knowledge is designed to condense deterministic pattern counts and to advance fault recognition probability by means of a similar nominal set of test points. Thus, the most recent structure is a combination of conservative scan chains and per-cycle-driven hybrid remark test points that capture defective items every shift cycle into enthusiastic scan chains, resulting in the introduction of assumed arbitrary trial patterns in a test-per-clock fashion. Thus, by identifying experiments inside the suggested system, industrial designers validate the feasibility.

B. Built-In Self-Test (BIST) with Power Constraints

A low-power (LP) scan-based BIST format, consisting of LP pseudorandom testing, LP deterministic BIST, and LP reseeding modes of applications, is developed to satisfy the demand for LP self-testing of digital circuits. This format is compatible with the power requirements for self-testing. One of the main things that this BIST architecture does is provide a low-power weighted pseudorandom test pattern generator. This generator uses weighted test-enable signals and a clock disabling scheme to cut down on unnecessary switching by selectively scan-enabling and reducing power consumption during test mode application[18]. To present industry-relevant designs according to the LP BIST architecture, a design-for-testability (DFT) mechanism is required. The DFT mechanism offers a shiny algorithm to either produce a sequence of degrade sub-circuits, given a weight fitted to all the sets of scan chains test-enable signals, and also the alteration of the weight in the direction of testability maximisation without breaching a desired power profile. A low-power-DLT approach where deterministic test patterns are encoded on random-pattern resistant fault models with only a subset of flip-flops being triggered in every clock cycle to minimise switching power cost.

C. Hierarchical and Modular DFT for Power Reduction

Hierarchical Design-for-Test (DFT) techniques offer an effective solution to the challenges associated with large and complex designs, such as increased tool memory requirements, longer runtimes, and limited pin accessibility [19]. This approach involves partitioning the chip into smaller, manageable modules or cores, enabling faster and more efficient test development and execution. As modern design flows already follow a core-based methodology for synthesis and physical design, hierarchical DFT aligns naturally with this structure. The growing availability of tool automation has further accelerated its adoption across the industry, making it a practical and scalable strategy for power-aware test integration.

Figure 2 illustrates a modular DFT architecture where test patterns are created at the core level, significantly reducing memory usage and runtime compared to full-chip testing. This approach enables early and parallel testing of individual cores, improving overall efficiency. The retargeting process mapping core-level patterns to chip-level pins is fast and lightweight. Additionally, this hierarchical DFT method helps reduce overall test time compared to traditional monolithic DFT strategies.

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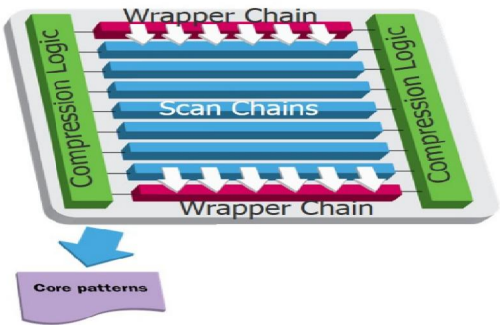

Fig. 2. DFT Completed for Each Core, Including Pattern Generation

IV. INTEGRATION OF POWER MANAGEMENT WITH TESTING

Most commonly used in microgrid (MG) and nano grid (NG) applications, Power management systems (PMS) balance between power demand and supply continuously by keeping the DC bus voltage constant. Equally, PMS applies to the enhancement of power-bound test efficiencies in digital circuit testing[20]. It would have the main aim of controlling the power consumed during testing in real-time, ensuring that the test power can be operated within the safe limits of the test environment [21]. Methods like test-aware power gating and dynamic voltage, frequency scaling (DVFS) can restrict the amount of power and switching activity that can be used during testing. However, power management services (volts support, power factor correction, and transient power management) are also possible, where a stable circuit performance is achieved when testing a circuit with the aid of a test cycle. A stringent environment limits stable testing due to several critical parameters, including voltage, energy and power, all of which have a direct influence on them.

A. Dynamic Voltage and Frequency Scaling (DVFS) during Test

The DVS is added to DFS to save even more energy. DVFS is a tried-and-true method that makes batteries last longer in handheld devices and drives down energy use in data centres. Voltage scaling can cut power use by a lot without affecting how things work [22]. Scaling voltage and frequency are good ways to make different types of computers work better while using less power. This part is mostly about figuring out voltage values, because not having enough operating voltage can make the microcontroller or microprocessor less useful and less stable. To figure out voltage numbers, use formula (1):

$$U_{DVFS}(f) - A \times e^{f/B}[V], \qquad (1)$$

The values and frequencies of the microcontroller power supply are used to find U_DVFS (f), where A=1.791011 and B=26.1804846. The datasheet for the microcontroller unit states that the frequency of 0.131 MHz requires the lowest power consumption, at 1.8 V. The same holds true for 16 MHz; 3.3 V is the power supply voltage.

B. Automatic Test Pattern Generation (ATPG)

The ATPG is a method for generating test vectors that can identify defects according to a predefined fault model. The goal is to create patterns that can distinguish between a fault-free circuit and one containing a specific fault. As described in Figure 3, a test pattern p for a stuck-at fault f is effective if it causes a discrepancy at one or more output nodes, meaning the outputs of the faulty and fault-free circuits differ under the same input conditions [23]. Although this example employs stuck-at fault model, the idea of creating output-observable differences is no less applicable to other fault types (transition delay and path delay faults, to name a few). ATPG is of utmost importance as the fault coverage needs to be high, the test generation time and the complexity of the computation need to be less.

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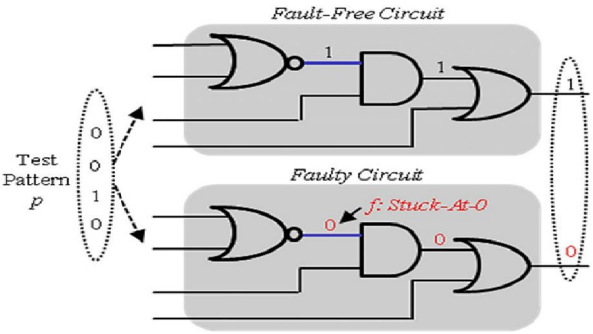

Fig. 3.Concept of Fault Detection

Figure 3 illustrates a stuck-at-0 fault in a digital circuit. In the fault-free circuit, the test pattern produces a correct output of '1', whereas in the faulty circuit, a line is stuck at '0', resulting in an incorrect output of '0'. This shows the method in which faults are detected by comparing certain test patterns with outputs.

C. Adaptive Testing with Power Monitoring

Adaptive certified power monitoring testing is an on-the-fly technique that adapts the testing procedure dynamically the circuit consumes power. Throughout testing, the power sensors built in the chip keep track of important variables like switching, current, and voltage [24]. When measured power crosses a set of predetermined limits, adaptive mechanisms are enabled to adjust the test flow that may include lowering the test clock frequency, disabling some scan chains temporarily, or delaying test patterns to avoid large current draw and possible test damage. The technique is safe and reliable, particularly in designs that are sensitive to power such as mobile and IoT devices [25]. Adaptive testing with real-time power feedback can be used to balance thermal influences and enhance fault coverage rate and minimize thermo-sensitivity-related false failure. In the context of modern VLSI circuits, this is effective because minimizing the peak power during test is very important in terms of device integrity and long life.

V. LITERATURE REVIEW

This literature survey offers power-limited testing methodologies in digital circuits, which include OPF optimization, power system stability and low power testing. It illustrates improvements in methods, challenges in practice and new trends of AI-driven, heuristic and hardware-friendly solutions.

Babiker et al. (2025) article has given a clear picture of Optimal Power Flow (OPF) that includes its basics, mathematical formulation and some of its variations, general concepts related to the OPF optimization problem and the different methods developed to resolve it. It also examines the way in which the techniques have developed beyond the classical ways to more complex and contemporary ways of approaching them which include mathematical approaches to the strategies of artificial intelligence like using metaheuristic and ML algorithms. Some of the families of the convex relaxation techniques have been discussed in this paper. Ultimately, issues, gaps, and fields that may need exploration are indicated in the paper. OPF problem has become more critical in design and operation of recent power systems[26].

Ali et al. (2025) paper introduces a distinction between fundamental and non-fundamental stability to cope with high penetration of RES. There is a further consideration of the presented methods that exist to test power system stability (PSS) during significant integration of RES in the study. It also points out key provisions of the integration of RES, network configuration, the evaluation and mitigation measures, and modelling tools adopted. PSS strategies are divided into three categories by the literature, including the model-based, and the use of AI. The review is aimed at providing academicians and professionals with in-depth understanding of PSS evaluation methods. Especially when it comes to PSS that possess more RESs integration involved it provides potential opportunities and insight into future research topics/areas of related concern.[27].

Li et al. (2024) provide the scan-based BIST of RSFQ circuits, performing response compression and pseudo-random pattern generation, providing at-speed capabilities in self-test. It introduces novel concepts and makes evident that the

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current pattern generator design is unsuitable for RSFQ. Create a new at-speed self-test control method based on the scan architecture. Demonstrate how innovative architecture makes testing easier with less overhead. To test these flaws, a scan architecture and an autonomous test pattern generator (ATPG) are developed. However, the test clock frequency is significantly decreased when test patterns and answers are transferred from the test apparatus at ambient temperature to the chip being tested in liquid helium using lengthy wires. At the same time, this technology's high clock frequency requires an at-speed test to assess delay issues[28].

Gonda and S. H (2023) article explains how a BIST architecture was developed and used in VLSI patterns to fulfill low-power purposes. The need to develop power-conscious design methodologies has been prompted by the increasing demand for energy-efficient electronic gadgets and the exponential growth of portable systems. BIST is a significant on-chip testing technique that helps to achieve the integrated circuit's dependability and quality. The implementation is carried out using the FPGA platform which proves that the proposed architecture is feasible and has practical use in bioinformatics. By using a complete BIST architecture, which considerably reduces power consumption during testing, this study improves the low-power VLSI design. The need to develop power-conscious design methodologies has been prompted by the increasing demand for energy-efficient electronic gadgets and the exponential growth of portable systems. The suggested design can be easily configured to fit the most significant numbers of low-powered VLSI applications and coupling with regular Verilog synthesis[29].

Abbasmollaei et al. (2022) paper unleashes a very configurable new approximation multiplier of unsigned integers. It tries to maintain accuracy and minimize all kinds of hardware parameters. Compared with the past benchmarks of the configurable algorithm, the proposed method has the most favorable solutions in the power-accuracy tradeoff. The wide range of power reduction options it provides from 35 to 85 percent meets the needs of most applications while staying within reasonable budgets. Additionally, the DCT has been applied using the suggested approximation multiplier. Approximate computing can solve these problems by enlarging the amount of computation on a limited power budget[30].

Priya and S (2021) paper compares scan power reduction techniques that are test-bound and heuristic in nature using the ISCAS89 benchmarking circuits. The proposed solution to the X-filling technique permits the power consumption to be reduced by 70 percent. Why? Because compared to a typical scan, the X-factor dropped to 0.57, a specific technology leads to a reduction in average power of 63.62 percent with respect to the shift component and 69.9 percent with regard to the capture component. VDSM has been incorporated into the new advances of VLSI. This has enabled the rapid growth of transistor density, with smaller, battery-powered, portable, high-performance, smart computer devices multiplying. Due to such drawbacks, power minimization becomes a vital prerequisite not only to test engineers but also to design engineers[31].

Table I summarizes recent advancements in power-constrained testing techniques for digital circuits, highlighting diverse methodologies, key findings, challenges, and future research directions across BIST, scan testing, and optimization approaches.

Table 1: Summary of a Study on Techniques for Power-Constrained Testing of Digital Circuits

Author	Study On	Approach	Key Findings	Challenges	Future Directions
Babiker et al. (2025)	Optimal Power Flow (OPF) and its optimisation	Mathematical formulation, conventional, metaheuristic, and AI-based methods	Comprehensive review of OPF types, solution methods, and convex relaxation techniques	Complexity of real-time OPF in modern grids with renewables	Advancing AI-driven OPF with real-time adaptation for smart grids
Ali et al. (2025)	PSS (Power System Stability) with a high	Classification of stability, model/optimisation/AI-based assessment	Framework for PSS under high RES, categorized evaluation	Managing diverse RES effects and ensuring	Developing unified, scalable PSS evaluation frameworks and

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	penetration of RES	techniques	methods	accurate simulation tools	robust simulation models for future grids
Li et al. (2024)	Scan-based BIST for RSFQ circuits	At-speed self-test, scan architecture, new control strategy	Low-overhead BIST design suitable for RSFQ circuits	Testing challenges due to extreme temperature and clock frequency constraints	Enhancing ATPG techniques for superconducting environments and high-speed testing
Gonda. et.al. (2023)	Low-power BIST for VLSI applications	FPGA-based implementation of power-aware BIST	Demonstrated feasibility and effectiveness of low-power BIST	Balancing power efficiency with testing coverage	Refining BIST architectures for newer VLSI technologies and IoT devices
Abbasmollaei et al. (2022)	Design of a configurable approximate multiplier for unsigned numbers	Developed a new approximate multiplier architecture with tunable parameters	Achieved high accuracy with significant power savings (35%–85%); effective in DCT-based applications	Balancing between configurability, accuracy, and power optimisation in real-time applications	Expand applicability to other DSP and AI domains; improve fault tolerance; explore adaptive configurations
Priya et.al. (2021)	Scan power reduction via X-filling	Heuristic X-filling approach with ISCAS'89 benchmarks	Up to 70% power reduction; effective shift and capture power savings	Integration of X-filling with industrial test flows	Enhancing heuristic algorithms for scan power reduction and evaluating in real-world VDSM circuits

VI. CONCLUSION AND FUTURE WORK

Power-constrained testing is essential in modern VLSI design due to the increased complexity, density, and power demands of circuits. Excessive power dissipation during test mode can cause circuit damage, reliability issues, and higher testing costs. This review discussed various techniques to address these challenges, including test vector optimisation, clock gating, scan chain methods, low-power DFT architectures, and adaptive testing with real-time power monitoring. Approaches like BIST with power constraints, hierarchical DFT, and DVFS effectively reduce switching activity and peak power during testing. Additionally, AI-driven test scheduling and metaheuristic optimisation enhance test efficiency in complex SoCs and 3D ICs. Integrating power management with testing enables safer, more reliable, and cost-efficient validation of digital systems. However, some methods introduce additional hardware complexity or longer test times. Moreover, ensuring scalability and seamless integration across various platforms remains a significant limitation that future research must address for broader industrial adoption.

Future research in power-constrained testing should integrate machine learning algorithms for intelligent test pattern generation and adaptive power control. Standardised low-power testing frameworks for emerging technologies like quantum computing, flexible electronics, and AI accelerators should be developed. Real-time power-aware testing in heterogeneous systems requires scalable and lightweight solutions. Advancements in on-chip power monitoring and collaborative DFT can create energy-efficient test environments.

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