IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 5, Issue 13, April 2025
Impact Factor: 7.67

Design of CMOS Based two Stage Operational Amplifier with Improved Design Parameters for Both Inverting and Non-Inverting Functionality Mode

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Abstract: *Operational amplifiers (op-amps) are fundamental components in analog and mixed-signal circuit design, with widespread applications in communication and medical systems. This project focuses on the design of a CMOS-based two-stage operational amplifier optimized for both inverting and non-inverting functionality. Utilizing 45 nm CMOS technology, the op-amp operates at a low supply voltage of 1V to reduce power dissipation. The design aims to achieve a high gain ($\geqslant$ 60 dB), a unity gain bandwidth that meets or exceeds required specifications, and a phase margin of $\geqslant$ 45 degrees to ensure stability. Key parameters such as gain, bandwidth, slew rate, gain margin, and phase margin are carefully optimized to enhance performance. The design methodology strikes a balance between performance and power consumption, offering greater flexibility than previous approaches.*
The proposed op-amp is simulated and analyzed using Microwind EDA software. Simulation results indicate a power dissipation of 319.766 µW and an occupied area of 10.9 µm². The open loop gain is 20.18 dB, with a gain margin of 14.07 dB and a phase margin of 94.26°, ensuring unconditional stability. The op-amp's performance under dynamic conditions is verified through transient analysis, confirming its suitability for low-power applications. The design meets modern VLSI technology demands by optimizing parameters like power consumption and area, making it highly suitable for use in advanced analog systems.

Keywords: CMOS, Operational Amplifier (Op-Amp), Two-Stage Design, 45 nm Technology, Microwind EDA, Analog Circuit Design, VLSI Technology.

I. INTRODUCTION

Operational Amplifiers (Op-Amps) are vital components in analog and mixed-signal circuit design, extensively used in signal conditioning, filtering, and data conversion. With the increasing demand for low-power, high-performance devices, CMOS technology has become the preferred choice for Op-Amp design due to its scalability, energy efficiency, and compatibility with digital systems.

This paper presents the design and analysis of a CMOS-based two-stage Op-Amp using 45nm technology, implemented and simulated in the Microwind EDA tool. The two-stage architecture was chosen to achieve high voltage gain and improved output swing, suitable for both inverting and non-inverting configurations. The design focuses on optimizing key parameters such as voltage gain, bandwidth, power dissipation, gain margin, and phase margin. Special attention is given to compensation techniques and transistor-level biasing strategies to ensure stability and enhance frequency response.

DOI: 10.48175/IJARSCT-26007

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The designed Op-Amp operates at a core voltage of 1.0V and I/O voltage of 1.8V, with simulation results showing an open-loop gain of 20.18 dB, phase margin of 94.26°, gain margin of 14.07 dB, and power dissipation of 319.766 µW. This study aims to provide an efficient and scalable Op-Amp solution for modern low-power applications.

II. LITERATURE REVIEW

Recent advancements in CMOS-based operational amplifiers (Op-Amps) have primarily focused on optimizing power consumption, improving gain, increasing bandwidth, and enhancing overall performance for modern analog and mixed-signal applications. With the growing demand for low-power and high-speed electronic devices, researchers have explored various CMOS technologies, architectures, and simulation platforms to meet evolving requirements.

Smrithi et al. (2024) designed a high-gain differential amplifier using 180nm CMOS technology, targeting low power consumption and improved performance. Their proposed Op-Amp achieved a gain of 60 dB with a power dissipation of 1.3 mW. The amplifier featured high input impedance and low output impedance, making it suitable for applications requiring precision amplification.

Srilakshmi et al. (2020) presented a dual-stage Op-Amp using 45nm CMOS technology. Their design achieved a notable gain of 72 dB, a slew rate of 122 V/µs, and a gain-bandwidth product of 4.60 MHz. The enhanced performance over single-stage designs highlighted the benefits of using multi-stage amplifiers for complex analog and mixed-signal environments.

Srilekha et al. (2020) conducted a comparative study on various Op-Amp architectures using 180nm technology in the Cadence Virtuoso platform. Their work analyzed different current mirror configurations and evaluated key parameters such as gain, power dissipation, and frequency response. The results provided valuable insights into how load structures affect Op-Amp performance.

Arun et al. proposed a compact, low-voltage CMOS Op-Amp operating in weak and moderate inversion regions using nonconventional modes of MOS transistors. Simulated using Mentor Graphics tools, their design targeted low-power and small-area applications, achieving higher slew rates and minimal silicon area, making it suitable for portable and embedded systems.

Kumar et al. (2019) introduced a cascode-based Op-Amp using 180nm CMOS technology. The amplifier demonstrated a DC voltage gain of 68.6 dB, a unity gain bandwidth (UGB) of 420 MHz, and a power dissipation of only 114 µW. It exhibited strong performance with a slew rate of 72.8 V/µs and a CMRR of approximately 102.6 dB. The design was implemented and verified using Cadence Virtuoso, showcasing its efficiency for high-speed analog circuits.

Richard E. Vallee and Ezz I. El-MasIy designed a high-performance Op-Amp using 3-micron CMOS technology with cascode current sources and an enhanced push-pull output stage. Their amplifier was developed for high-frequency switched-capacitor (SC) filter applications, achieving a gain of 72 dB and a unity gain bandwidth of 40 MHz with a bias current of 100 µA and load capacitance of 15 pF.

Hatim Ameziane et al. proposed a CMOS Op-Amp design based on Adaptive Biasing Circuitry (ABC) using 1µm FDSOI CMOS technology. The design operated at a 3.75V power supply with a 70 µA bias current and achieved a low power dissipation of 0.62 mW. The use of weak inversion operation enabled significant energy savings, making it suitable for ultra-low-power systems.

Shashidhara et al. (2018) developed a two-stage Op-Amp using 0.18µm CMOS technology optimized for low power and high-speed performance. The amplifier operated at 1.8V supply, consumed only 5 µA of current, and achieved 87 dB gain with 75 µW power consumption. Additionally, it offered a unity gain bandwidth of 4.87 MHz and a slew rate of 4.126 V/µs.

Nagulapalli et al. demonstrated a robust Op-Amp design using 65nm CMOS technology, simulated in Spectre. Their design achieved a gain of 60 dB and a bandwidth of 10 MHz while operating at a low supply voltage of 0.8V. Impressively, the design consumed only 205 µA current and occupied a minimal silicon area of 0.002464 mm², outperforming traditional folded cascode Op-Amps at lower voltages.

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III. METHODOLOGY

The proposed work focuses on the design and simulation of a two-stage CMOS-based operational amplifier using 45nm technology in the Microwind 3.9 environment. The objective is to achieve an efficient low-power Op-Amp with improved parameters such as gain, bandwidth, phase margin, and slew rate for both inverting and non-inverting operation modes.

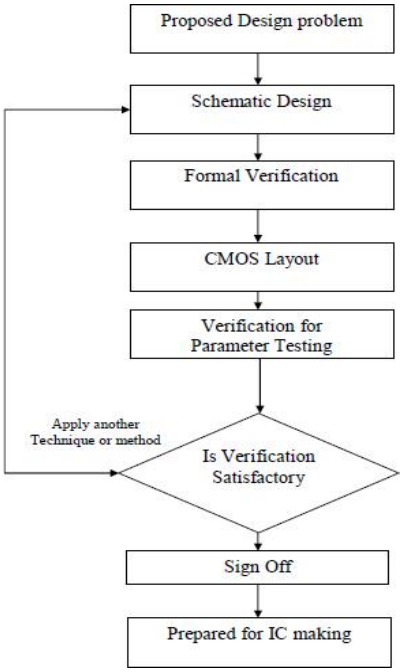

Figure 1. Flowchart representing the design and analysis steps for CMOS Op-Amp implementation.

Design process begins with schematic development using CMOS transistors modeled with BSIM4. This is followed by performance verification through DC and AC simulations to extract key parameters like voltage gain, power dissipation, and stability margins.

Once the schematic is verified, a physical layout is created using Microwind, incorporating design constraints like area, parasitics, and device matching.

The layout undergoes physical verification and parametric analysis to ensure design correctness and performance consistency. If any parameter fails to meet the target specification, the design loop is repeated with updated strategies

The methodology also includes a comparative analysis between the proposed design and existing literature to highlight improvements. The ultimate goal is to create a layout-ready Op-Amp design optimized for IC fabrication and suitable for integration in low-power analog applications.

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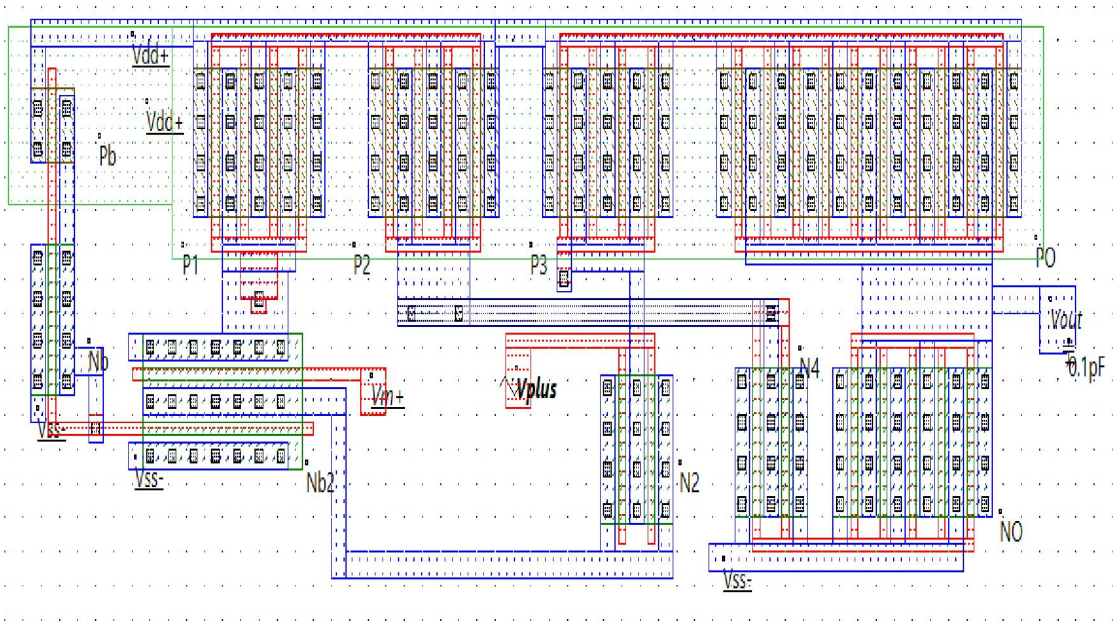


Figure 2. Physical layout of the proposed CMOS two-stage operational amplifier designed using Microwind 3.9.

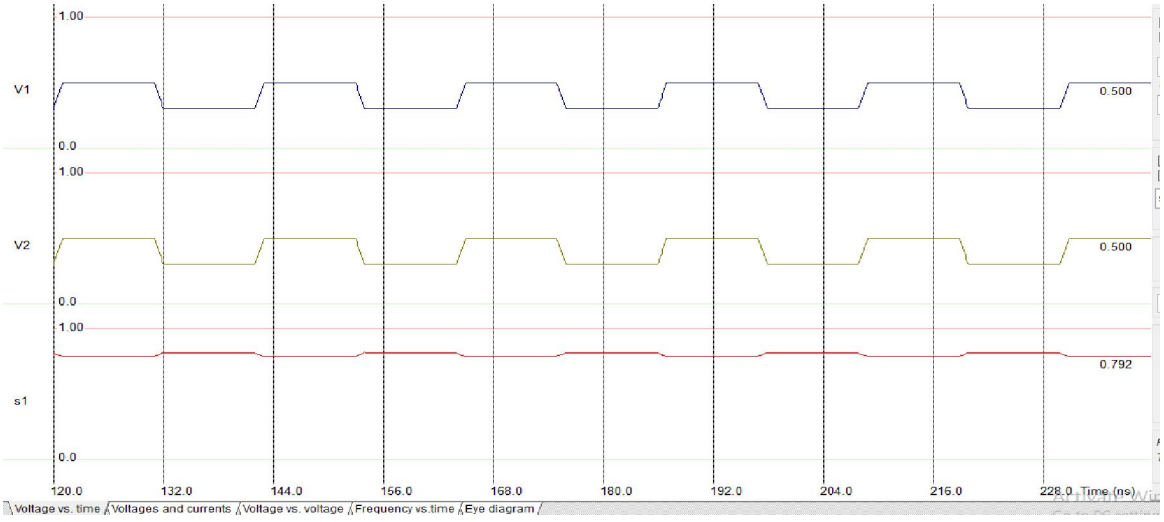
IV. RESULTS AND DISCUSSION

The performance of the proposed CMOS-based two-stage operational amplifier was evaluated using the Microwind 3.9 EDA tool with 45nm CMOS technology. Key simulation tests were conducted on the differential amplifier, current mirror, and OP-AMP in both inverting and non-inverting modes.

A. Differential Amplifier

Simulation verified that when both inputs are equal (V1 = V2), the output is approximately zero, confirming high CMRR. For unequal inputs (V1 > V2), an amplified output is observed.

Figure 3. Simulation result of differential amplifier for V1=V2



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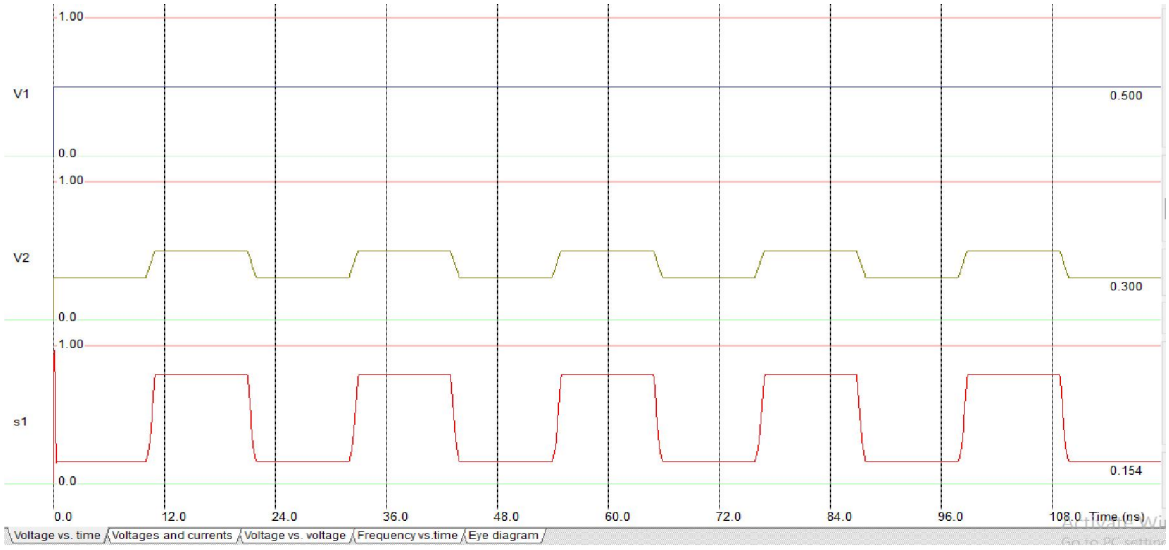

Figure 4. Simulation result of differential amplifier for V1>V2

B. Current Mirror

Using layout-based simulation, the current mirror showed consistent current replication across both branches. I2 remained approximately 5 µA, validating the design's accuracy and symmetry.

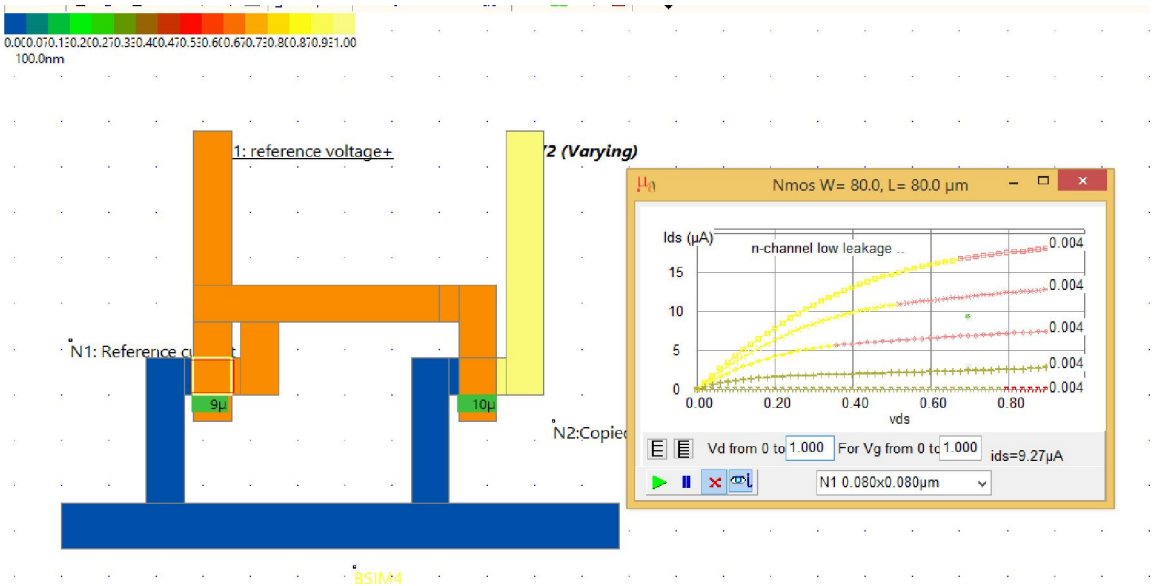

Figure 5. Simulation on layout for current Mirror circuit

C. OP-AMP in Inverting & Non-Inverting Mode

The inverting mode simulation showed a gain of **20.18 dB** and good transient response. In non-inverting mode, the bandwidth improved and the amplifier achieved a **gain margin of 14.07 dB** and a **phase margin of 94.26°**, indicating unconditional stability

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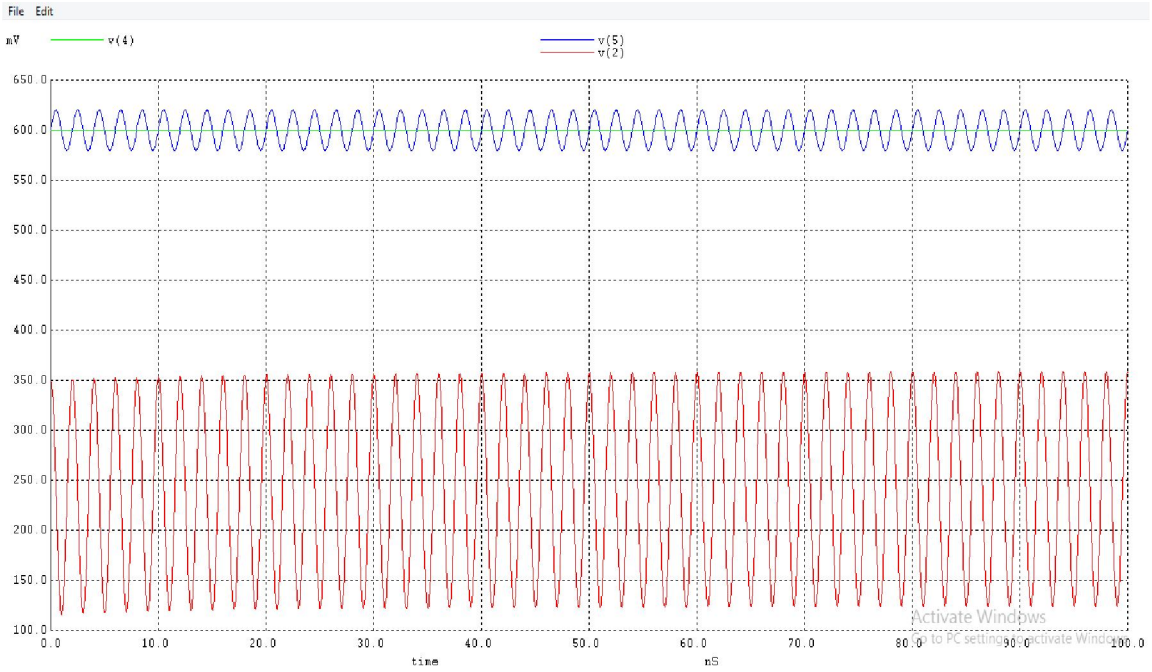

Figure 6. Transient analysis OP-AMP in Inverting Mode Operation

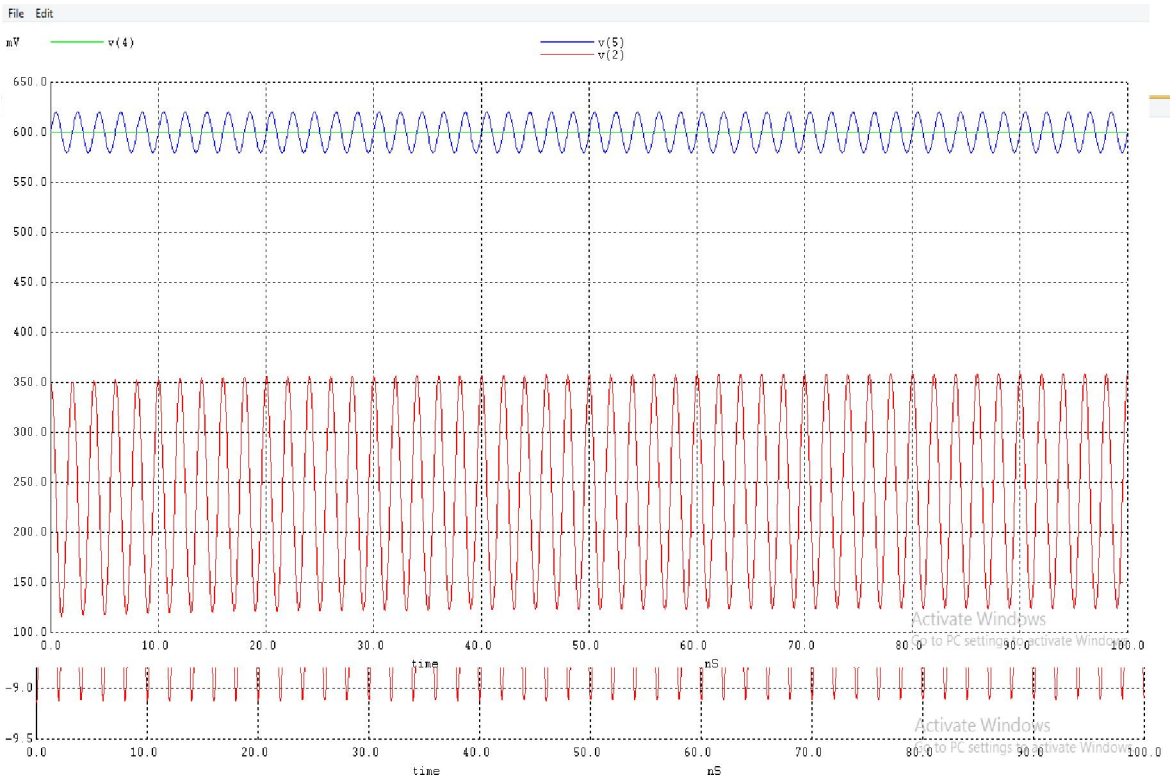

Figure 7. Transient analysis OP-AMP in Non-inverting Mode Operation

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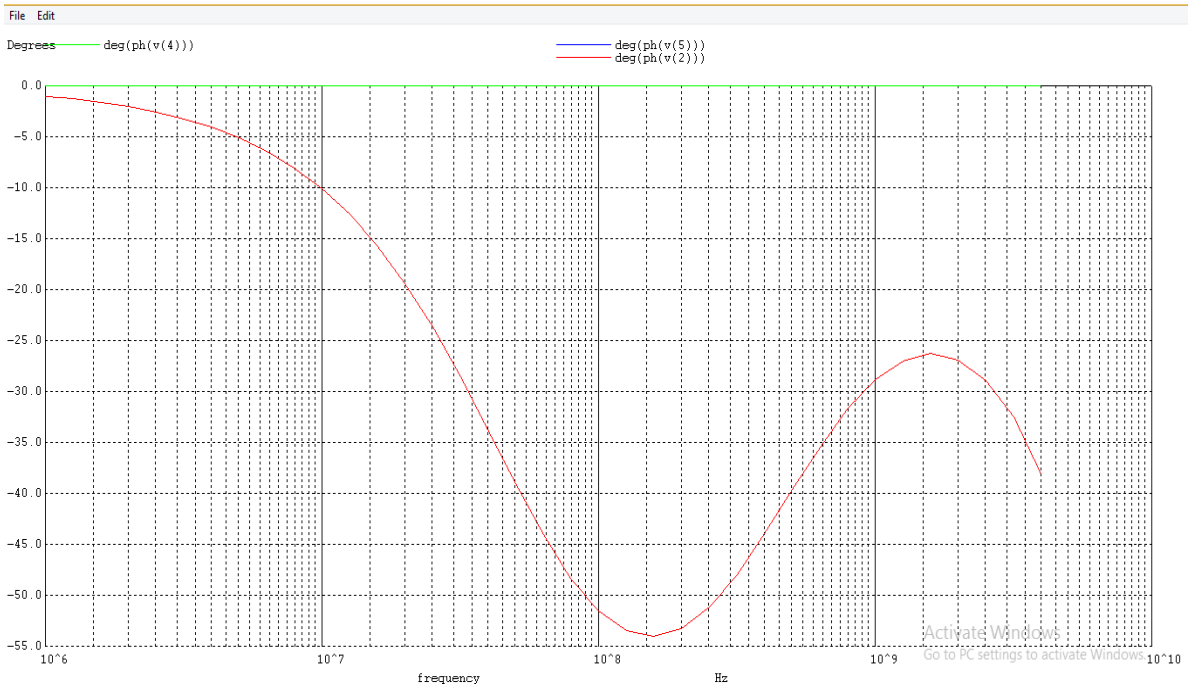

Figure 8. Phase Margin for OP-AMP

D. Layout-Level Analysis

Transient simulations of the physical layout confirmed proper operation. Maximum current observed (IDmax) was **0.337 mA**, and power dissipation was **307.970 µW**

V. CONCLUSION

In this research, a CMOS-based two-stage operational amplifier was successfully designed and simulated using 45nm technology within the Microwind EDA environment. The primary objective was to achieve improved performance parameters—such as gain, bandwidth, phase margin, and low power consumption—while maintaining reliable operation in both inverting and non-inverting configurations.

The simulation results confirm that the proposed Op-Amp achieves an open-loop gain of 21.18 dB, a unity gain bandwidth of 6.31 MHz, a gain margin of 14.07 dB, and a phase margin of 94.27°, ensuring unconditional stability. The total power consumption was observed to be only 307.970 µW, with an occupied area of 10.9 µm², making the design highly efficient and compact.

The successful layout-level validation and low power profile demonstrate that the amplifier is well-suited for integration in modern analog and mixed-signal systems, particularly in power-sensitive applications such as IoT devices, portable electronics, and sensor interfaces. The results highlight the effectiveness of using optimized biasing, scaling techniques, and compensation strategies in advanced CMOS design.

REFERENCES

[1] S. V., D. S. S. Sam, and G. Manoj, "Design and Analysis of Two Stage Op-Amp in 180nm CMOS Process," 2024 7th Int. Conf. on Devices, Circuits and Systems (ICDCS), Coimbatore, India, 2024, pp. 253–257, doi: 10.1109/ICDCS59278.2024.10560977.

[2] S. R. Madabhushanam, L. Malladi, and S. R. Gudepu, "Design of High Gain Dual Stage Operational Amplifier using CMOS 45nm Technology," 2020 4th Int. Conf. on I-SMAC, Palladam, India, 2020, pp. 1184–1188, doi: 10.1109/I-SMAC49090.2020.9243590.

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[3] S. Kothapalli et al., "Comparative Experimental Analysis of Different Op-Amps using 180nm CMOS Technology," 2020 Int. Conf. on Emerging Trends in Information Technology and Engineering (ic-ETITE), Vellore, India, 2020, pp. 1–6, doi: 10.1109/icETITE47903.2020.440.
[4] A. Katara, R. Balwani, P. Wagh, and P. Salankar, "Design of OP-AMP Using CMOS Technology & Its Application," 2016 Int. Conf. on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, India, 2016, pp. 3633–3636, doi: 10.1109/ICEEOT.2016.7755384.
[5] K. Sai Kumar et al., "Implementation of a CMOS Operational Amplifier using Composite Cascode Stages," 2019 5th Int. Conf. on Advanced Computing & Communication Systems (ICACCS), Coimbatore, India, 2019, pp. 689–693, doi: 10.1109/ICACCS.2019.8728335.
[6] R. E. Vallee and E. I. El-Masry, "High Performance CMOS Operational-Amplifier," IEEE Int. Symp. on Circuits and Systems, Portland, OR, USA, 1989, vol. 2, pp. 1475–1478, doi: 10.1109/ISCAS.1989.100636.
[7] H. Ameziane, K. Zared, and H. Qjidaa, "New CMOS OP-AMP Design with an Improved Adaptive Biasing Circuitry," WSEAS Trans. on Circuits and Systems, 2020, doi: 10.37394/23201.2020.19.27.
[8] K. Shashidhara, S. R. Ijjadab, and B. Nareshb, "A 75 µW Two-Stage Op-Amp using 0.18µm CMOS Technology for High-Speed Operations," APMAS 2018 – Int. Conf. on Applied Physics and Materials Science.
[9] R. Nagulapalli et al., "A Low Voltage Opamp Based on Current Mirror Technique for Bio-medical Applications," 2018 3rd IEEE Int. Conf. on Recent Trends in Electronics, Information & Communication Technology (RTEICT), Bangalore, India, pp. 901–904, doi: 10.1109/RTEICT42901.2018.9012265.
[10] K. T. Tan, N. Ahmad, and M. M. Isa, "Design and Analysis of Two Stage CMOS Operational Amplifier Using 0.13µm Technology," AIP Conf. Proc., vol. 2203, no. 1, p. 020040, 2020, doi: 10.1063/1.5142132.
[11] N. V. Butyrlagin et al., "Design Features of High-Speed CMOS Differential Difference Operational Amplifiers at Low Static Current Consumption," 26th TELFOR 2018, Serbia, Belgrade, Nov. 20–21, 2018.
[12] E. Sicard and S. Bendhia, Basics of CMOS Cell Design, Tata McGraw-Hill, India.
[13] E. Sicard and S. Bendhia, Advanced CMOS Cell Design, Tata McGraw-Hill, India.
[14] H. Saini and S. Suman, "Analysis of Different Single-Stage Amplifiers," Mody Univ. Int. J. of Computing and Engg. Research, vol. 1, no. 2, pp. 100–103, 2017.
[15] V. S. Suman, K. G. Sharma, and P. K. Ghosh, "Design of Ring Oscillator Based VCO with Improved Performance," Innovative Systems Design and Engineering, vol. 5, no. 2, pp. 31–41, 2014, doi: 10.1109/Acct.2015.127.
[16] B. Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2001.
[17] A. Sedra and K. Smith, Microelectronic Circuits: Theory and Applications, New Delhi: Oxford University Press, 2009.
[18] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, 3rd ed., New Jersey: John Wiley & Sons, 2010.
[19] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 3rd ed., New York: Oxford University Press, 2012.
[20] W. Jung, Op Amp Applications Handbook, Oxford: Newnes Elsevier, 2005.
[21] Analog Devices, "CMOS Analog Design Basics," [Online]. Available: https://www.analog.com/en/education/education-library/cmos-analog-design.html
[22] IIT Bombay, "Two-Stage CMOS Op-Amp Design Concepts," [Online]. Available: https://www.ee.iitb.ac.in/~chetan/courses/AnalogCircuits/opamp2stage.pdf
[23] Microwind EDA Tool, "Design and Simulation Using Microwind Tool," [Online]. Available: https://www.microwind.net/
[24] YouTube, "CMOS Op-Amp Design Tutorial," [Online]. Available: https://www.youtube.com/watch?v=cgPYzjk6iEk