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Analysis of Asymmetrical 31-Level Cascaded Inverter with SICPWM using ANFIS Controller for Solar PV Applications

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Abstract: *The modified topologies for a asymmetrical cascaded inverter is analyzed with a smaller number of DC voltage sources, power electronic knobs, and power diodes which can generate several levels. The Adaptive Neuro-Fuzzy Inference System (ANFIS) is suggested for asymmetrical modified cascaded inverter topologies to decrease the Total Harmonic Distortions (THD). This technique forbids the changes present in the performance from the modified inverter voltage. The purpose of this research effort is to demonstrate that the significance of ANFIS is to integrate learning to alter the substance of knowledge that meets the learner's needs. The ANFIS model concert calculates using necessary error quantities that display the perfect location required for an improved conviction. For the THD evaluation with and without ANFIS controller, the analysis of thirty-one-level for asymmetrical design was performed. ANFIS controller will be used to obtaining the controlled Root Mean Square (RMS) output from the voltage. The performance of without controller and with ANFIS controlled 31-level asymmetrical cascaded inverter is evaluated and compared with the use of MATLAB/Simulink.*

Keywords: Cascaded Inverter, Root Mean Square Value, Total Harmonic Distortion, Adaptive Neuro-Fuzzy Inference System

I. INTRODUCTION

Multilevel inverter performs as a significant part in medium-voltage and high-power applications. About its performance, the idea after the multi-level inverter will be able to extract greater than two levels and offers several advantages[1], such as an increase in output voltage range. This multilevel inverter explicitly incorporates its ability to analyze using series-connected semiconductor components at greater DC voltages[2]. Several multilevel inverter topologies, such as diode-clamped technology or neutral point-clamped (NPC) were introduced in 1980, though advanced topologies introduced in the 1990s.

The conventional multi-level inverter topologies like flying capacitor inverter (FC), and neutral-point clamped Inverter (NPC) use a single common source where multiple isolated DC sources have used as a cascaded multilevel inverter topology[3]. In diode clamp technology, a single DC source used, but the clamp diode requirement is exceptionally high. In flying capacitor topology, capacitors placed in the location of clamping diodes. Consequently, the control turns to intricate with the rise in the inverter's total size [4]. The cascaded multi-level inverter topology is chosen because of its modular environment, being flexible with an ideal location and facilities to protract. Using the same circuit components can increase the no. of voltage measures produced at the output can be improved by appropriately selecting the DC voltage sources[1]. If all DC sources' value is equal, then it is called symmetrical and asymmetrical cascaded inverter topology[5].

The THD is comparatively superior for a traditional two-level voltage converter that produces the organization issue with the voltage, and it decreases the life-cycle of the electric installation automation[6]. Utilizing a filtering circuit

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could solve the power inverter output issue that makes it more difficult for the realization and enhances the cost[7]. Following the multi-level inverter, the proposed cascaded inverter will be able to alleviate this issue to generate an improved execution of the output from a voltage as well as the less THD without any high-volume filter. By employing the appropriate network structure, can reduce the THD substantially.

The analysis of proposed cascaded inverters consisting of 31-level for asymmetrical design is detailed, and subsequent results with and without controller are discussed and also handles the ANFIS controller, step response calculation, and THD analysis for asymmetrical cascaded inverter topology, and corresponding results discussed.

II. MODIFIED 31-LEVEL ASYMMETRICAL CASCADED INVERTER TOPOLOGY

Fig.1 illustrates the circuit of 31-level asymmetrical cascaded inverter topology of the proposed system. In this topology, the integration of H-bridge and modular structure is discussed. The switches and DC voltage sources vary appropriately to obtain the multilevel outputs in a modular configuration, whereas the H-Bridge must be kept on the same. By raising the DC supply voltage and switches in the modular configuration as well as cascaded them with the H-bridge unit, the output of the supply voltages can be raised. The Asymmetrical cascaded Inverter for 31-level is analysed. In this configuration, the Super Imposed Carrier Pulse-width-modulation (SIC-PWM) method had to generate the inverter circuit for producing signals. The switching frequency is fs=2KHz. This PWM method provides the multi-level inverter self-balancing property.

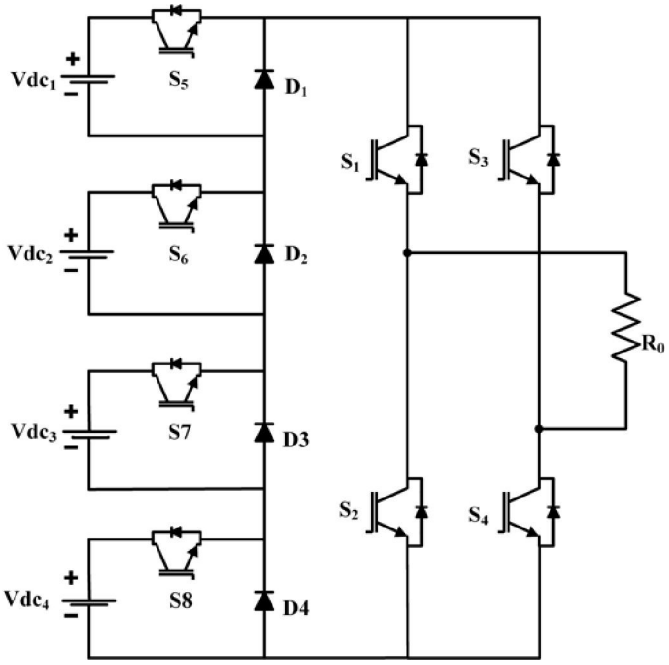

Fig. 1 31-level Asymmetrical inverter

As demonstrated in the Fig.1, a simple block of modified 31-level cascaded inverter topology was comprised of the DC voltage [8]. Whether the magnitude of the DC supply sources is not the same, then the inverter is called the asymmetrical cascaded Inverter [11]. It will be able to easily enhance the maximum output and increase the dc operating voltage and achieves various modifications in switches and cascading them with the h-bridge unit [12]. Source of DC voltage, including a linear sequence by a component of two-or three, were identified. The dc source voltage can be expressed by 'n' and Vdc as 2(n-1) Vdc.

$$Vdc_1 = Vdc, Vdc_2 = 2Vdc, Vdc_3 = 4Vdc \ldots Vdc_n = 2^{(n-1)}\,\text{Vdc} \quad (2)$$

The arrangement of the asymmetrical inverter has a +ve group and -ve group. The +ve group is performing for delivering +ve signal wave beyond load capacity and the amount of gain voltage Vdc rises with the rise in the switch. In circuit alignment, The voltage output 0Vdc is produced whenever the switches (S1, S3) are in the turned-on state and

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(S5, S6, S7, S8, S2, S4) are turn off. The +Vdcvoltage output is produced whenever the switches over (S5, S1, S4) are in the turned-on state and (S6, S7, S8, S2, S3) are turned off. The voltage output +2Vdc is produced whenever the switches (S6, S1, S4) are in the turned-on state and (S5, S7, S8, S2, S3) are turned off. The voltage output +3Vdc is produced whenever the switches (S5, S6, S1, S4) are in the turned-on state and (S7, S8, S2, S3) are turned off and son for +15Vdc. The voltage output -Vdc is produced whenever the switches (S5, S2, S3) are in the turned-on state and (S6, S7, S8, S1, S4) are turned off. The -2Vdc voltage output is produced whenever the switches over (S6, S2, S3) are in the turned-on state and (S5, S7, S8, S1, S4) are turn off. The -3Vdc voltage output is produced whenever the switches over (S5, S6, S2, S3) are in the turned-on state and (S7, S8, S1, S4) are turned off and son for -15Vdc.The switching pattern for 31-level cascaded inverter is as shown in Table.1

Table. 1. Switching pattern for 31-level cascaded inverter

Switching states		**Output voltage (V0)**
Switching states Turn ON.	**Switching states Turn OFF.**	
S5, S6,S7,S8, S1, S4	S2, S3	+15Vdc
S6, S7, S8, S1, S4	S5, S2, S3	+14Vdc
S5, S7, S8, S1, S4	S6, S2, S3	+13VdC
S7, S8, S1, S4	S5, S6, S2, S3	+12Vdc
S5, S6, S8,S1, S4	S7, S2, S3	+11Vdc
S6, S8, S1, S4	S5, S7, S2, S3	+10Vdc
S5, S8, S1, S4	S6, S7, S2, S3	+9Vdc
S8, S1, S4	S5, S6, S7, S2, S3	+8Vdc
S5, S6, S7, S1, S4	S8, S2, S3	+7Vdc
S6, S7, S1, S4	S5, S8, S2, S3	+6Vdc
S5, S7, S1, S4	S6, S8, S2,S3	+5Vdc
S7, S1, S4	S5, S6, S8, S2, S3	+4Vdc
S5, S6, S1, S4	S7, S8, S2, S3	+3Vdc
S6, S1, S4	S5, S7, S8, S2, S3	+2Vdc
S5, S1, S4	S6, S7, S8, S2, S3	+Vdc
S1, S3	S5, S6, S7, S8, S2, S4	0
S5, S2, S3	S6, S7, S8, S1, S4	-Vdc
S6, S2, S3	S5, S7, S8, S1, S4	-2Vdc
S5, S6, S2, S3	S7, S8, S1, S4	-3Vdc
S7, S2, S3	S5, S6, S8, S1, S4	-4Vdc
S5, S7, S2, S3	S6, S8, S1, S4	-5Vdc
S6, S7, S2, S3	S5, S7, S8, S1, S4	-6Vdc
S5, S6, S7, S2, S3	S8, S1, S4	-7Vdc
S8, S2, S3	S5, S7, S6, S1, S4	-8Vdc
S5, S8, S2, S3	S6, S7,S1, S4	-9Vdc
S6, S8, S2, S3	S5, S7, S1, S4	-10Vdc
S5, S6, S8, S2, S3	S7, S1, S4	-11Vdc
S7, S8, S2, S3	S5, S6, S1, S4	-12Vdc
S5, S7, S8, S2, S3	S6, S8, S1, S4	-13Vdc
S6, S7, S8, S2, S3	S5, S1, S4	-14Vdc
S5, S6,S7,S8, S2, S3	S1, S4	-15Vdc

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III. ANFIS CONTROLLER BASED MODIFIED CASCADED INVERTER

ANFIS design envisioned in Figure.16. It is synthesis configuration which combines the educational skills of Artificial Neural Network (ANN) [13]. An excellent experience presentation and reasoning skills of fuzzy sense that possess the abilities to change over the starring position of the association to accomplish the desired output[14]. An adaptive network may thought to know the FIS that combines practically all the types of neural network simulations[15]. ANFIS uses the hybrid-educational rule while at the same time achieves modern programs for rule-making or diagnostic procedures. ANFIS was being set up as both an essential part for fine-tuning the membership functions parameters of Fuzzy inference systems [16].

ANFIS is modest information provided by the education technique that dues a fuzzy inference scheme ideal to transform a consented work into the target efficiency. This forecast includes membership rules, if-then rules and fuzzy logic operators. Instead, two kinds of fuzzy schemes are typically labelled as the Mamdani and Sugeno models. The following five essential data handling cycles in ANFIS operation comprise a fuzzy operative application, input fuzzification, request for technique, output expansion, and defuzzification. ANFIS is usually a multi-layered back-propagation system where each and every device perform a particular role on inbound signals(node function)[16]. The one output ' z ' and ' x ' and ' y ' are two responses measured for the case. assume that in the rule-base, there are Takagi and Sugeno type of fuzzy if-then rules of in the rule base.

Rule 1: IF x = A1, y = B1; THEN f1=P1x+Q1y+R1

Rule 2: IF x = A2, y = B2; THEN f2=P2x+Q2y+R2

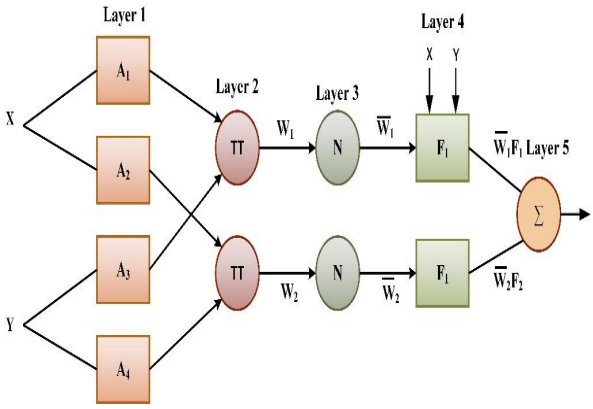

Figure 16: ANFIS Architecture

IV. RESULTS AND DISCUSSION

The modified asymmetrical 31-level cascaded inverter using the Super Imposed Carrier Pulse width Modulation (SICPWM) technique is modelled in MATLAB/Simulink. The analysis was carried out without a controller and with an ANFIS controller.

Simulation results 31-level modified cascaded inverter Without controller

Using the MATLAB/Simulink the modified asymmetrical 31-level cascaded inverter using the SICPWM technique is simulated.

The following are the 31-level modified asymmetrical inverter simulation parameters considered for R-load:

Input voltage (DC)=30V (Vdc1=2V, Vdc2=4V, Vdc3=8V, Vdc4=16)

Carrier switching frequency *fs* = 2 KHZ

R-Load = 100 Ω

From the Figure.1, four input voltage sources Vdc1, Vdc2, Vdc3 and vdc4 is considered for the thirty-one-level cascaded inverter. The 31-level asymmetrical inverter is shown in Fig.2. For each source, the input voltage is Vdc1 = 2V; Vdc2 = 4V; Vdc3 = 8V; Vdc4 = 16V. Then The load-wide output voltage is 29.80V (RMS voltage is 21.07V). The load-wide output voltage is shown in Figure.3. The current through the load is 0.298A. Fig. 13 Depicts the current

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through the load. The FFT evaluation of thirty-one-level symmetrical inverter is illustrated in Figure.4. The THD value from the FFT is 5.40%.

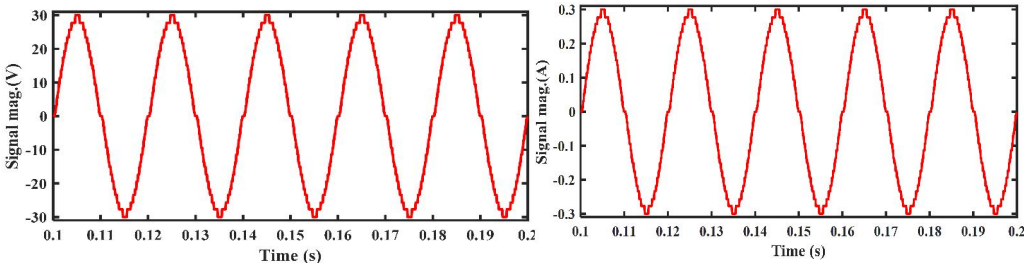

Figure 14: The load-wide output voltage for Figure 15: Output Current through the load thirty-one-level inverter

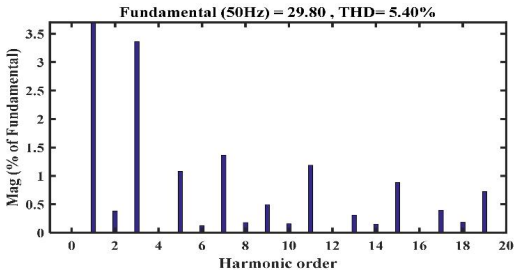

Figure 15: Thirty-one-level inverter FFT analysis

Simulation results 31-level modified cascaded inverter Without controller

To control the RMS output voltage of asymmetrical cascaded Inverter. The initial reference voltage is maintained as 14V and then increased after 1sec to 22V. The pulse width is lower in the starting element of the voltage (when the 14V of voltage is gained) and the increases pulse width after 1seconds to 22V to maximize voltage output. It is also obtained the RMS value of a modified inverter using ANFIS controller.

Those analyses are taken for the 31-level asymmetrical inverter wit ANFIS Controller. The Result analysis for Asymmetrical Inverter with ANFIS controller is illustrated in Figure.17 and Figure.18.

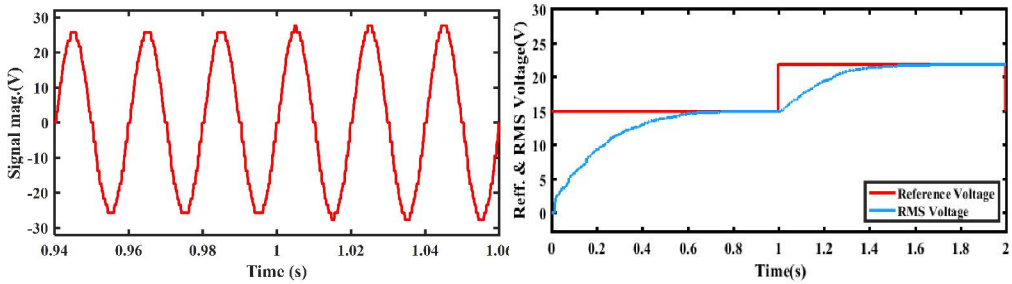

Fig. 113. Output voltage across the load **Fig. 112.** Reference and Output RMS voltage

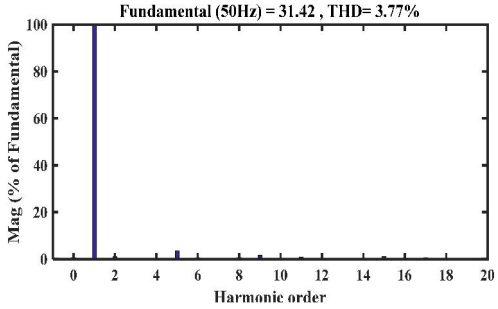

Fig. 114. FFT analysis

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THD for Asymmetrical Cascaded Inverter

Table 4 shows the THD of cascaded inverter with and without ANFIS controllers for different levels. From the table 4, it can be observed that the THD is decreased steadily by an increase in the number of levels in both the symmetrical and asymmetrical inverter topology and also represents in charts as shown in Figure.21 and Figure.22.

Table 4: THD comparison for and Asymmetrical Cascaded Inverter

Asymmetrical cascaded inverter		
Levels	**Without controller (ANFIS)**	**With controller (ANFIS)**
31-level	5.40%	3.77%

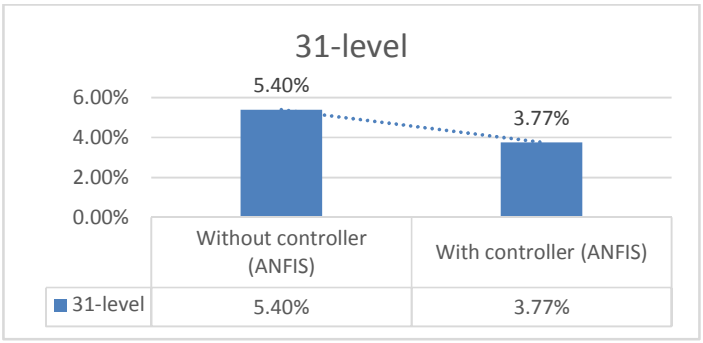

Figure 21: FFT analysis of Asymmetrical cascaded Inverter

V. CONCLUSION

This paper defined demonstrating the important variations in THD percentage with minimal no of switches by adjusting the modification of circuit for asymmetrical configuration of 31-level inverter topology. The evaluation of circuit modification for 31-level of the modified inverter is performed for both with and without ANFIS controller. ANFIS control methods are maintained to offer improved performance following the method on the inverter to control the RMS the voltage output and to remove the harmonic content. The perspective of this approach is referred, and THD outcomes are being the comparison for the various modified inverter. This research shows the potential significance of ANFIS with fusion learning. The way of characteristic error quantities has computed the execution of ANFIS.

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