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Conditional Bridging Low-Power High-Speed Sense-Amplifiers Over Flip-Flops

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Abstract: *Along with space and speed, power consumption is regarded as a significant difficulty in contemporary VLSI design. The flip-flop is an integral part of digital systems. We compare and contrast four distinct flip-flop topologies in sub-threshold operation: IP-DCO, MHLFF, CPSFF, & CPFF. These topologies encompass both pulse-triggered and conditional techniques. Sub threshold technology has recently made it feasible to implement applications with very low power consumption. This technology's benefit is that it reduces the power consuming flip-flops. When operating at the same frequency, a sub threshold circuit uses less power than a strong inversion circuit. The 18nm technology used by Tanner in cmos is used for design. At a power supply voltage of 1V, the flip-flops are examined from every angle, and characteristics including average power, power delay product, and power delay are measured.*

Keywords: Sub Threshold Technology, Flip Flop, Low Power

I. INTRODUCTION

Increases in clock frequency and tightening of timing standards are necessary to meet the need for electronic systems to operate at high speeds [1]. In order to meet the necessary timing requirements, these systems have used high-speed circuits, leading to significant power consumption. The prevalence of mobile electronic equipment in modern life has also increased the need of energy-efficient calculations [2, 3]. While speed performance may be sacrificed, low-power design strategies such as voltage scaling to reduce switching power and conditional operations to avoid redundant power may be used to deal with energy restrictions [4, 5]. It is common practice in high-performance mobile apps to intentionally sacrifice some power in exchange for faster processing times. State transitions and synchronised data flow are governed in synchronised digital integrated systems by flip-flops and latches. The maximum operating frequencies are determined by the timing-critical signal routes that often include flip-flops, making their high-speed design crucial [8]. The importance of low-power flip-flop design has grown in recent years due to the fact that a single processor may employ millions of flip-flops [9], with their combined power consumption reaching 20–40% of the overall power [9], [10], [11]. Consequently, a crucial concern in the design of high-speed mobile electronic systems is the reduction of power consumption and delay caused by the use of flip-flops & latches, which are not easy to achieve simultaneously. The master-slave topology of the transmission-gate flip-flop (TGFF) [12] (FIGURE 1) allows it to provide modest power consumption and data-to-output (DQ) delay in synchronous digital integrated circuits. Power savings via voltage scaling is another advantage that may be gained from TGFF's dependable operating in the near-threshold voltage (NTV) area. In TGFF, so-called pulse-based approaches are able to reduce the DQ latency because the sampling and capturing of input data are separated in the master and slave stages, respectively [13], [14], [15]. One such implementation is the transmission-gate pulsed latch (TGPL) [13], which combines a pulse generator with a single latching step. Reduced DQ latency is achieved by eliminating the master stage in TGFF and immediately transferring input data to the output within a small pulse period caused by the clock edge. In spite of its fast functioning, TGPL may use a lot of power because of the circuit overhead required to generate the short pulse. In addition, the pulse width's unpredictability as a consequence of process variables might lead to problematic functioning, particularly in the NTV zone. While new circuit approaches have helped with pulse generation in some cases, maintaining internally delayed local clocks for pulsed operations still results in higher overall power consumption than TGFF [14], [15]. The

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employment of the sense-amplifier-based flip-flop (SAFF) method is another approach to increasing the speed of timing components [17]. Fast sampling and input data capture at the triggering clock edge are achieved by the flip-flop via the use of a symmetric latch and a differential precharged circuit in the first stage, respectively, allowing for high-speed operation. Altering the latching stage's architecture may increase power and speed even more, but it can also lead to undesirable signal fighting, which compromises latency and power consumption [18]. Additionally, these flip-flops are vulnerable to increasing variability in the NTV area since they use a weak shorting mechanism to guarantee static functioning. Despite the fact that the issue may be resolved by monitoring the arrival of precharged nodes, there are significant power and latency overheads. This work introduces conditional bridging flip-flops (CBFFs), which are based on sensing amplifiers and may improve speed while lowering power consumption. Problems with the previously mentioned shorting device are eliminated by the suggested conditional bridging method, which does not incur any power or speed overheads. A single-ended version (CBFF-S) of the flip-flop is suggested for decreasing power consumption, while a differential version (CBFF-D) is suggested for lowering latency. In addition to being fast, low-power, and contention-free, CBFFs can reliably operate in the NTV zone.

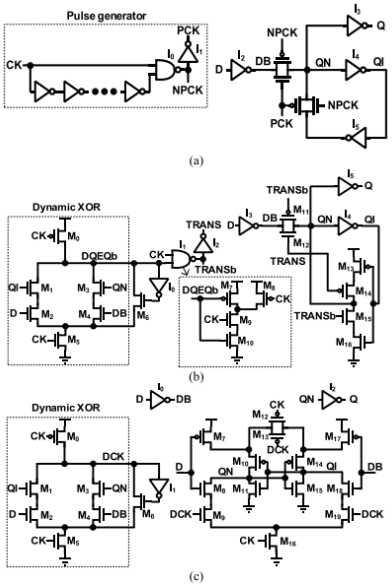

Fig: 1. A) TGPL [13], (b) STPL [14], and (c) DCPL [15] are pulsed latch-based FFs.

II. EXISTING METHOD

2.1. SENSE-AMPLIFIER-BASED FLIP-FLOP

A. CONDITIONAL BRIDGING

A conditional bridging approach is suggested as a more power-efficient way to fix problems with the reducing device (M4) in traditional SAFFs. Motivated by the idea that the shorting device should only be activated when D changes after being collected by Q, the goal is to eradicate any relevant redundant transitions. In other situations, it is more prudent to disable the device in order to avoid the drawbacks of using an ineffective device and to avoid the unnecessary discharge of an internal node (X or Y) on the opposite branch. Figure shows the SA stage with a conditional bridging circuit, where the shorting device is driven by the circuit's output (CBG). The suggested conditional bridge circuit monitors the values of D, DB, SB, & RB to switch on M4 when CK=1 only when D changes & becomes different from Q. Because SB & RB are pre-charged high when CK is low, activating M13, M17, and maybe one of M12 & M16, keeping CBG low is independent of the D value. Depending on the value of D, SB or RB discharge at the rising edge of the clock. Assuming SB is discharged, keeping CBG low by M16 – M17 is possible with D=RB=1. As soon as D goes low, CBG rises high via M14 and M15, enabling the activation of M4 to supply a DC route to the ground and guaranteeing static functioning.

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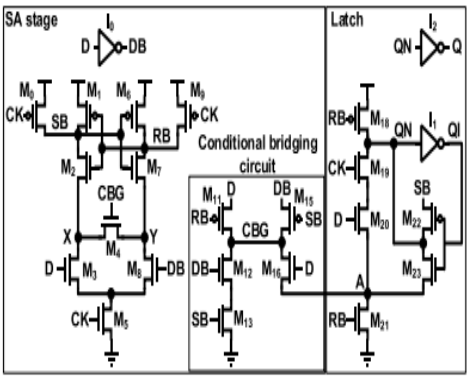

Fig:2. A flip-flop that just has one side open is another option.

B. STRUCTURE AND OPERATION

Two variants of the conditional-bridging flip-flop (CBFF) are suggested, both of which use the conditional bridging mechanism that was previously discussed. A sensing amplifier stage (M0-M9 and I0), a conditional bridging circuit (M11-M16) and a single-ended latch stage (M18- M23, I1, & I2) make up the single-ended version (CBFF-S), as shown in Figure 5. A reduction in the overall number of transistors in the flip-flop is achieved by modifying the conditional bridging circuit. More specifically, D drives M11's sources and DB's sources directly, whereas M15's sources are driven via DB. In Figure 5, the latch merges M21 and M17, which were controlled by RB in Figure 4, are shown. The glitch- & contention-free single-ended latch, powered by the SA stage without inversion (as indicated on the right portion of Fig.), allows the latching stage to be optimised for power consumption and device count. M18 uses just RB to pull-up QN following the rising clock edge, whereas M19–M21 uses only RB to pull-down QN. The purpose of inserting M20, which is driven by D, is to remove QN glitches caused by the precharged high value of RB at the beginning of the clock high frequency. In order to draw down QN without contention, SB is employed to drive the source of M22. Node A is likewise linked to the source of M23 so that QN may be pulled up without conflict. The lack of a pulsed operation distinguishes the latching stage of CBFF-S shown in Fig. from that of conventional pulsed latches [13], [14], [15].

Choose CBFF-S if you care about operational reliability, latency, and power usage. One way to avoid unnecessary CBG transitions is to control when the conditional bridging logic engages the shorting device (M4). At low switching activity, the conditional bridging circuit will minimise power consumption because it transitions when D changes after Q grabs D during CK=1. The circuit allows for miniaturisation by reducing power consumption and preventing shorting. To save power, CBFF-S only releases the opposing precharge node (X or Y) if D changes, as D seldom changes under low input switching activity. Regular SAFFs charge and discharge them on a clock cycle, as previously mentioned. The smallest possible shorting device might potentially decrease latency and draw out timing-critical impulses like SB and RB quicker due to its smaller parasitic capacitance. Disabling the shorting device allows for faster input sampling by eliminating SB-RB signal interference. Through direct control of the latching process, RB eliminates signal inversion and contention, hence decreasing clock-to-output (CQ) time. Pulling down precharged nodes reliably at low supply voltages is made possible by reducing congestion in the SA stage. CBFF-S's contention-free latching stage & conditional-bridging SA stage ensure input data is securely gathered while the system operates steadily in the highly volatile NTV zone. Presented here is the differential suggested flip-flop, often known as CBFF-D. Figure 13 shows two transistors, M13 and M30, that may be combined in the conditional bridging circuit without the need to add a third transistor because of the symmetric differential structure. When we add a few transistors after latching and remove the output inverter (I2 in Fig.), we can tell SB and RB to drive difference outputs Q , QB. Putting CK-powered M24 in parallel to pull-up keepers transistors M22 and M25 speeds up output pull-down by stopping them from struggling. While a setup comparable to the single-ended variant (M22 powered by SB in Fig) performs well at normal supply voltages, the inclusion of a delayed transistor (M24) is necessitated due to reliability concerns highlighted by Monte-Carlo simulations in the worst corners. In terms of operation speed and power consumption, CBFF-D is identical to its

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single-ended predecessor. Despite having a slightly higher overall power consumption owing to the bigger load capacitance of CK utilised to operate the differential latch, CBFF-D greatly decreases power usage in low-activity switching scenarios with its conditional bridging function. Due to the SA the stage's outputs driving Q and QB different latches, CBFF-D can outperform CBFF-S in terms of speed.

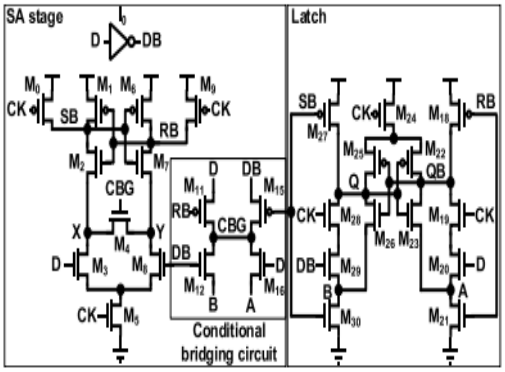

Fig:3. The suggested flip-flop in its differential form.

III. PROPOSED FLIP FLOP DESIGNS

3.1 CONDITIONAL BOOSTING AMPLIFIER

To improve its performance in collecting input data, a conditional boosting flip-flop uses conditional boosting methods. It is a kind of flip-flop circuit. Each input and output signal's logic state determines which boosting operations this flip-flop applies. In order to optimise its functioning for diverse input data circumstances, the conditional boosting flip-flop integrates output-dependent presetting and intake-dependent boosting concepts. This method minimises power usage during regular operation while allowing for speedier data gathering when needed. Capacitor terminals N and NB preset voltages are defined by outputs Q and QB to enable output-dependent presetting, as shown in Figure 4(a). The left-hand figure in Figure 4(a) shows that N is set to low and NB is set to high when Q is low & QB is high. On the flip side, N is set to high and NB to low when Q is low and QB is high (also referred to diagram in Fig. 4(a)). As seen in Figure 4(b), a nMOS transistor connects the non inverting input (D) to NB for input-dependent boosting, and another nMOS transistor links the inverting input (DB) to N. As seen on the left side of Figure 4(a), capacitor presetting may occur if the flip-flop stores low data. In this scenario, as seen in the top left figure of Figure 4(b)), a high input pulls NB to ground, which in turn boosts N towards -VDD via capacitive coupling. On the other hand, as shown in the bottom left schematic of Figure 4(b)), a low input would normally link N to ground. However, because to the node's setting to VSS, virtually no voltage change would occur at NB, resulting in no boosting. In the alternative case, as shown in the right-hand diagram of Figure 4(a)—capacitor presetting occurs when the flip-flop stores high data—a low input pulls N to ground, which in turn boosts NB towards -VDD via capacitive coupling—as shown in the bottom right-hand diagram of Figure 4(b).

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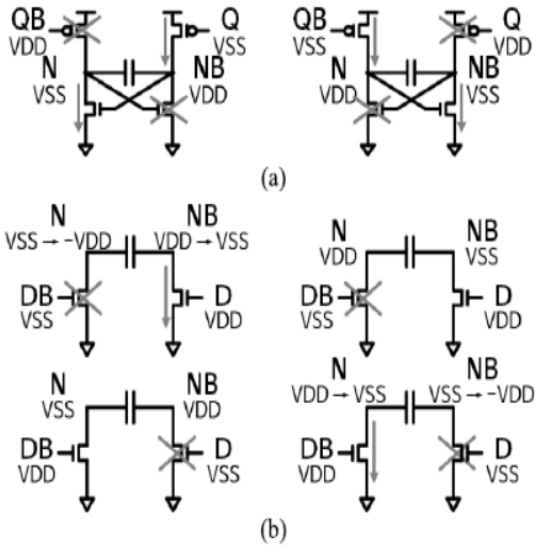

Fig 4: Block schematics for (a) data-dependent presetting of outputs and (b) data-dependent boosting of inputs.

	input (D)	output (Q)	boosting node (N)	boosting node (NB)
output-dependent presetting	-	VSS	VSS	VDD
		VDD	VDD	VSS
input-dependent boosting	D=VDD	VSS	VSS → -VDD	VDD → VSS
		VDD	VSS	VDD
	D=VSS	VSS	VDD	VSS
		VDD	VDD → VSS	VSS → -VDD

Fig 5: Findings for various Q and QB out puts

An explicit short pulse generator, a symmetric latch, and a conditional-boosting differential stage make up the system. Figure 6(a) shows the conditional-boosting differential stage in action. For output-dependent presetting, we use MP5, MP6, and MP7, and MN8 and MN9. For input-dependent boosting, we use MN5, MN6, and MN7 in conjunction with the boosting capacitor CBOOT. Figure 6(b) shows the symmetric latch, which consists of MP8–MP13 and MN10–MN15. A unique explicit pulse generator, as illustrated in Figure 6(c), is used to create a short pulsed signal PS, which is used to activate specific transistors inside the differential stage. The suggested pulse generator is different from traditional ones since it does not use a pMOS keeper. This leads to faster processing times and lower power consumption because signal fighting is eliminated during the pull-down of PSB. When introduced in tandem with MN1, MP1 plays the job of the keeper by helping to quickly bring down PSB and keeping its logic value high. During the rising edge of CLK, MN1, MP1, & I1 quickly discharge PSB, which causes PS to become high. After I2 and I3 have elapsed, MP2 charges PSB, which causes PS to go back to low and causes a short positive pulse at PS, the width of which is dictated by the latency of I2 & I3. Even though MP2 is not doing anything during CLK's low phase, MP1 is holding PSB high. Our analysis shows that with the same pulse widths and slew rates, reduced energy consumption of up to 9% are possible.

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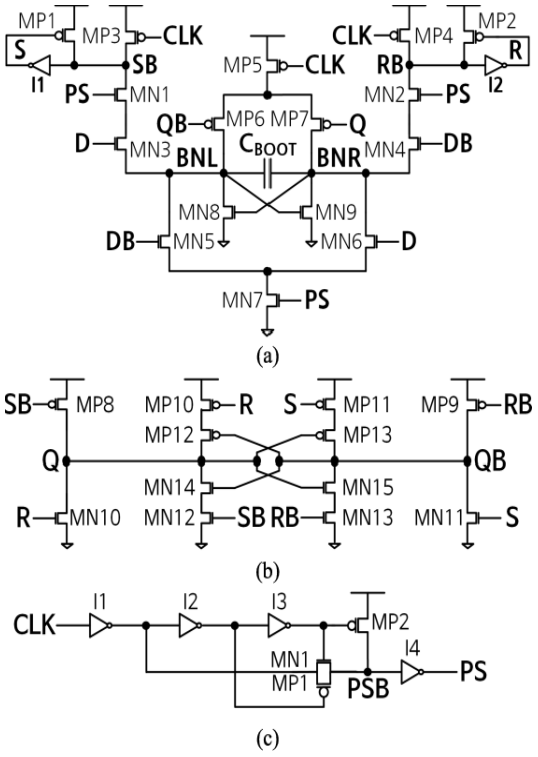

Fig:6. Presented as a possibilities CBFF. (a) The threshold for conditional-boosting differentials. (b) Latch is symmetrical. (c) A generator of explicit short pulses.

Delay, which is dependent on parasitic capacitances, and other power consumption issues may be circumvented by removing them. The figure displays the variance in the delay time of flip-flops. Based on the graph, it is evident that MHLFF has a lower latency than other flip-flops. Figure displays the typical amount of electricity that a flip-flop consumes. Among our four flip-flop designs, CPSFF has the lowest average power usage while MHLFF has the most. Compares the power delay product. The changes in the average power for different kinds of flip-flops. Compared to other flip flops, CPSFF has a lesser value. Among these four flip-flops, CPSFF provides the best performance.

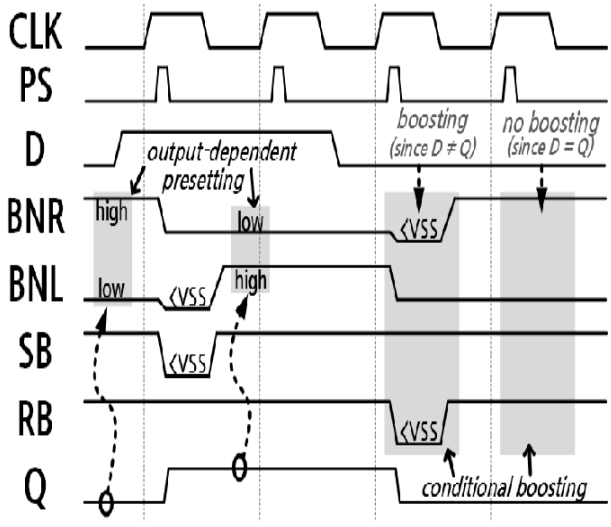

Fig: 7. The suggested flip-flop's timing diagram.

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IV. RESULTS

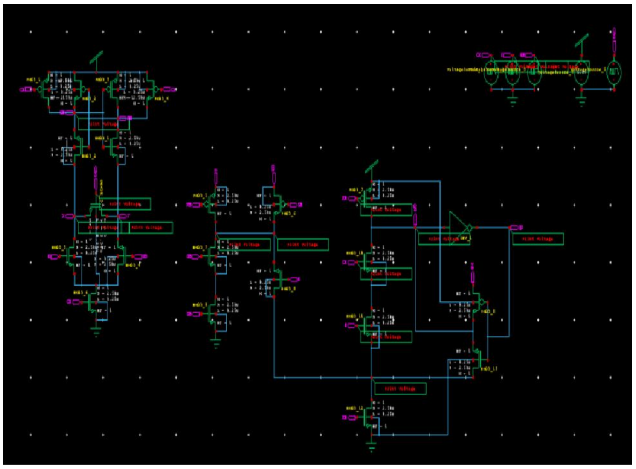

Fig:8. Existing schematic Single-ended version flip-flop

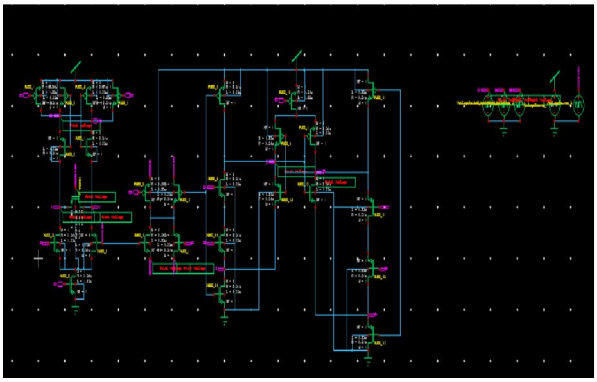

Fig:9. Existing schematic Differential version flip-flop.

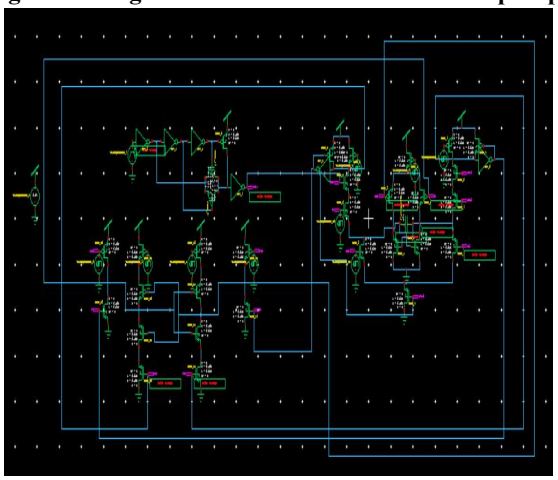

Fig:10. Schematic of Proposed Conditional Boosting Flip flop.

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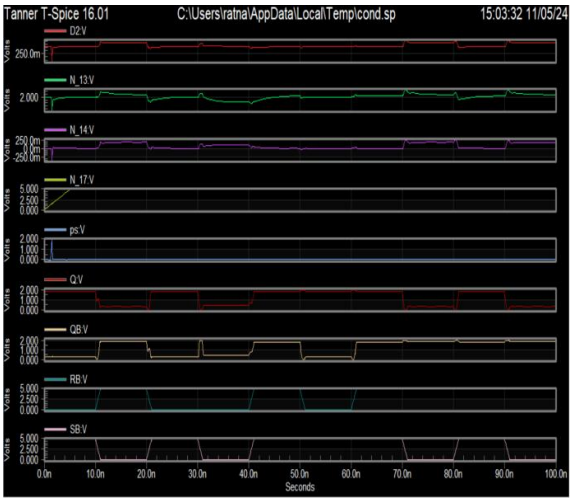

Fig 11: Amplified output waveform.

Averaging 8.1984W, the system's power usage trends were all over the place. During this time, power usage varied from 0.00000W at the lowest to 1.7371W at the highest. A setup time of 0.03 seconds was reported for the system to stabilise, which is in close agreement to the DC operating point. The system's settling into a steady state was indicated by a transitory phase lasting 0.39 seconds, according to further investigation.

4.1 PERFORMANCE COMPARISON:

Parameters	Existing method	Proposed method
Min Input Power	4.736 W	0.0000 W
Max Input power	7.6304 W	1.7371 W
Avg Input power	6.2587 W	8.1984 W
Delay	0.95 sec	ec

V. CONCLUSION

Reliable, high-performance, and low-power flip-flops based on sense amplifiers are presented in the work. To ensure static operation without redundant transitions, the shorting device is adaptively activated by the suggested conditional bridging. As a result, the effective capacitance parasite along the signal pathways that are timing-critical may be reduced by making the shorting device as small as possible. Directly driving the locking step without glitches or conflict significantly reduces power consumption and delay. A redesigned latching stage is used by the single-ended variant of the suggested flip-flop to optimise power consumption and space. The differential version, which includes a differential latching step, is also introduced to optimise performance and facilitate differential operation. Not only do the suggested flip-flops have better power and latency performance, but they can also stably function down to the NTV area. The suggested flip-flops showed promising results in a performance study conducted using an 18-nm CMOS technology, suggesting they might be useful in low-power, high-speed digital applications. An innovative constrained bandgap filter (CBFF) has been suggested for aggressively voltage scaling to the area around the threshold voltage without significantly reducing performance. With the help of a boost body driven scheme, this project presents a pulse trigger FF design that is ideal for low power applications. The idea of a multibit flip-flop coupled with a conditional boosting flip-flop is finally presented, allowing for the effective enhancement of power area and latency.

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