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An Analysis of Low-Power Design Strategies in Embedded Systems

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Abstract: *Every electrical device nowadays uses integrated CPUs. Power management is one of the biggest design problems in contemporary electronics. All power management strategies aim to maximize system performance within the power budget. High-end embedded processors have made mobile devices nearly as numerous as the world population. However, these advances have made power tracking these devices harder. Embedded system designers developed many power management solutions. Besides analyzing several research works on power management methodologies for embedded systems, this review article underlines the necessity for power management. This study aims to help academics and embedded system developers understand power management techniques and build more power-aware design strategies for future embedded systems.*

Keywords: Power Gating, Low-Power Design, Battery Management

I. INTRODUCTION

Embed systems are computers having software built into the hardware to do a particular purpose. Physical platforms that run application software and peripheral devices with ports are embedded systems. CPUs, memory, and communication channels make up the hardware platform. OS and application programming are software implementation. Controlling system power dissipation improves efficiency.

Recent years have seen a boom in embedded system features and applications. Wireless data, internet browsing, phone, and multimedia applications are on mobile embedded devices. New advancements emphasize power control more. As is known, mobile device users practically equal the global population. This hinders embedded system designers from creating a high-performance, low-power solution.

Power management in embedded devices and energy efficiency studies are covered in this article. This study emphasizes power management to inspire embedded system designers and researchers.

The document format is this. Section II discusses embedded system power management history and need. Section III addresses power management, where embedded system designers must optimize power. Section IV classifies and describes embedded device power management. Future editions conclude Section V.

II. BACKGROUND

Many embedded devices may become mobile convergence devices. Mobile convergence devices need plenty of computing power to provide many functionalities. However, many embedded mobile devices use batteries with limited energy. Managing power consumption while meeting all function throughput requirements is a major challenge in building embedded mobile devices.

Power determines whether an embedded system is portable or non-portable. Portable Embedded Systems with low power and good performance are difficult to design. DVD players, digital cameras, and mobile phones are embedded systems.

Power management in embedded systems is critical for several reasons.

Small Size and Battery Life

Power supply is essential for battery-powered mobile embedded devices. Heat from device power consumption is problematic in many Embedded Systems. System size also limits heat dissipation.

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Reaching Performance Requirements

Currently, embedded processors run resource-intensive tasks like multimedia processing. Recent embedded processors have multi-cores, multi-level caches, etc. to meet performance needs. Many embedded system areas use multicore architectures. The design of embedded systems has become power-efficient due to these improvements.

Ensuring Longevity

As indicated, temperature increase may double gadget failure rates. This illustrates that power dissipation affects embedded device dependability, which may be important for medical and mission-critical equipment.

III. OVERVIEW

Designers of power-optimized embedded systems must address three basic power concerns.

- Power Measurement
- Power Analysis
- Power Management

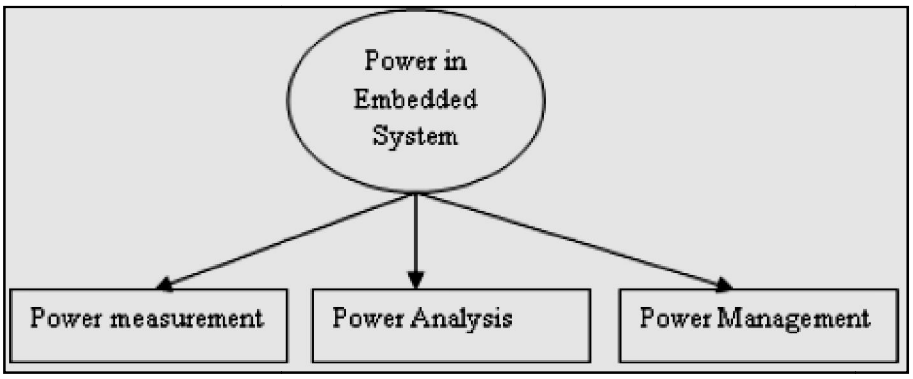

Figure 1: Power Concern in Embedded System

1. Power measurement

Most embedded devices measure power hardware or software. Software uses simulation models to assess power, whereas hardware measures CPU, communication channels, memory units, and peripheral device power. Simulations are preferred over hardware because they may be executed at numerous levels.

To measure, assess, and manage complex embedded systems in real time, Liang-Bi Chen et al. recommended real hardware power measurement using ARM-based SOC development boards and a power analysis platform. A case study revealed how this platform can assess a Digital Still Camera (DSC)'s power use and enhance power efficiency by dynamically considering quality and energy.

2. Power analysis

Measurement, experimentation, estimate, and approaches are used to analyze and verify system power usage. Power analysis models CPU, memory, and peripheral power use. Research on electricity use has been popular for years. Any power-saving method must monitor system power to make a judgment. Examples of this research are given. Jason Flinn et al. created Power Scope to monitor mobile app energy utilization. Based on program section power usage, Power Scope may assess energy consumption. Tested the technology on an adaptive video-payer to minimize energy use.

3. Power Management

Power management is any function on an electronic device that lets consumers control power consumption without affecting performance. Power management lets devices move between power modes with variable power use and performance characteristics.

Power management is a key challenge in embedded system design. Die thermal characteristics are unstable, system performance suffers, and power consumption rises. This makes power consumption sometimes more critical than

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system speed. Power management in embedded systems design may occur at chip, architectural, application, and system levels. System-level power management strategies are important because intelligent power-awareness reduces power consumption better than low-power design.

IV. POWER MANAGEMENT TECHNIQUES

Power management systems are grouped by their principal power-saving method.

- DVFS (Dynamic voltage and frequency scaling)
- Dynamic Power Management (DPM)
- Architecture level power management
- Application level power management

This section discusses many power management methods connected to the categorization.

Dynamic Voltage & Frequency Scaling:

DVFS adjusts electronic system voltage and frequency for performance and power. This approach involves changing voltage levels to system components during runtime to decrease power consumption while maintaining throughput. System power consumption is generally measured using this equation:

$$P=CV^2f \quad (1)$$

where P is power utilized, C is switching capacitance, V is supply voltage, and f is operating frequency. Adjusting voltage-frequency couples controls power consumption. Several commercial embedded processors feature power-saving DVFS. To achieve the desired power and performance, voltage and frequency pairings are tuned within established values. Figure 2 illustrates DVFS for a dual-core CPU.

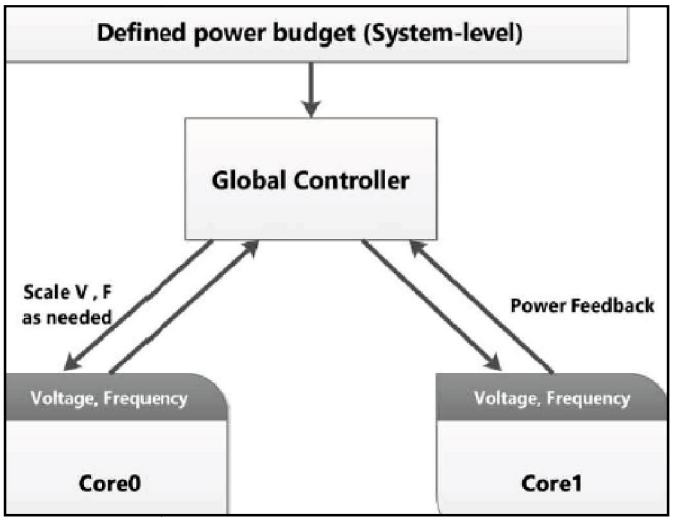

Figure 2: DVFS applied to a Dual-core processor

System-level controllers limit global on-chip controller power. Global controllers monitor core voltage, frequency, and power. These parameters instruct the global controller when to modify voltage and frequency. DVFS is used by most embedded system processors instead of general-purpose programs. Hua et al. showed how DVFS may conserve electricity in embedded computing systems and real-time applications. Explored energy reduction for trustworthy, deadline-driven real-time applications. Checkpointing, DVFS, and backward failure recovery maintain application dependability and deadlines.

DVFS-based energy optimization in real-time embedded systems was proposed by Quan et al. The best voltage schedule for a variable voltage processor-based real-time system with fixed-priority workloads was examined. Variable voltage processors may reduce energy use in many real-time embedded applications.

Edward Khan et al. used mathematical optimization to find energy-aware processor frequencies for soft real-time embedded systems. Assuming a fixed frequency range, mathematical models determined work frequency. Selecting

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nearby frequencies less and greater than the required frequency and employing some to satisfy real-time deadlines was the proper decision. With several deadlines, this strategy boosted job performance.
DVFS algorithms for each core in chip-multiprocessor (CMP) systems maximize energy, say Kim et al. They examined DVFS overheads, voltage transition time, and advantages in a 4-core multiprocessor with on-chip voltage regulators.

Dynamic Power Management:
Dynamic power management controls policy. These rules monitor system run-time activity to remove inactive components to save power. Every embedded system component saves electricity by using varied amounts and returning to normal at different periods. Within performance loss limits, idle low-power mode, resource reduction, etc. may increase system energy usage. Policy controls component function. Putting components in different operating modes with different performance and power consumption may increase electronic system power use with any power management technique. Policies set component operating modes based on system history, workload, and performance. Several dynamic power management policies are investigated.
Back propagation and RBF ANN were recommended for dynamic power control by Lu et al. Used these two approaches to greatly cut IBM mobile disk system power. Hybrid Dynamic Power Management by Wai-Kong Lee et al. estimates portable embedded system idle time. MA, TDNN, and random walk predict inactivity. We explored these methods on portable embedded devices since human usage behaviors impact device load. Learning-based multi-core processor DPM framework by Rong Ye et al. Learning-based job allocation reduced CPU idle. DPM power and performance were evaluated on 4- and 8-core embedded systems. Experimental results show learning algorithm DPM policies work.
Hwang et al.'s anticipatory power management evaluates application-specific I/O device utilization. The method compares stored and current execution patterns to forecast I/O accesses. Run programs and compare results to test the method. Parallelized OpenMP-based dynamic power management for multi-core embedded CPUs was presented by Chung et al. A preferable way counts app runtime cores. Turning off unnecessary cores saves energy. Both Intel Quad Core and ARM-11 MPCore worked. To lower AMD Quad-Core Opteron average active power, W. Lloyd Bircher et al. enhanced hardware and OS. OS management and hardware flexibility may degrade multi-core embedded processor power and performance. Balanced active-to-idle transitions conserve power and performance.

Architecture level power management:
For embedded system energy optimization, several researchers have devised architectural-level power management solutions. CPU cores, device drivers, memory, registers, bus protocols, clock gating, online profiling-based monitoring and control, and others save power via dynamic reconfiguration. M. Kinage et al. created a COTS dual-core soft core CPU. They optimized the design to conserve energy using XPA to investigate core power utilization. For disk-less, battery-powered embedded computers, Lei Yang et al.'s online RAM compression works effectively. They intended to increase RAM without hardware redesign while maintaining performance and energy efficiency. Linux kernel module virtual memory compressed swapped pages.
A power-efficient instruction re-execution processor microarchitecture was proposed by Emil Talpes et al. To reuse computations from previous implementations where possible. Long-term pipeline architecture front end downtime conserved power by re-executing acquired, decoded, executed, and retitled instructions. Experiments demonstrate execution cache size reduces and improves power. Yi-Ying Tsai et al.'s TrCache reduces instruction access CPU power. They recommend recycling pipeline back-end retired instructions to speed up embedded processors and save power. Transmission of additional TR cache instructions boosts instruction rate.
Samira Ataei et al. created Power-efficient transistor-based SRAM memory architecture for embedded multimedia applications. To lower retention mode leakage current, read and write static noise margin is increased. The voltage scaling of pixel data in photo and video apps saves power. Energy-efficient design decreases system power waste, said Massoud Pedram. Research delivers low bus encoding for embedded system power optimization. Power and performance are limited by processor-memory data transfer.

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Application level power management:

Multimedia and power-aware algorithms save electricity at the application level. Applications usually decide how to turn off or wake up system components. Active apps know how system resources are used. Apps alone decide power-managed systems' optimum user experience. Apps and consumers benefit transparently from these application-level embedded system power solutions. This lets user-focused apps see how users use the system to achieve their goals. Ahn et al. showed CPU bandwidth control-based application-specific power management. The suggested governor adjusts DVFS processor bandwidth to optimize CPU consumption. Multimedia application experiments imply CPU bandwidth management may maximize embedded system power and user experience.

Daniel Llamocca et al. created a GPU and FPGA 2D FIR filter for image and video processing. System accuracy and energy efficiency were assessed. In this application, FPGAs are slower than GPUs but utilize less energy. Yi-Chu Wang et al. demonstrated how to accurately map a smartphone platform to a facial recognition software for energy savings and performance. They evaluated if changing program algorithmic parameters and leveraging mobile CPUs and GPUs more would improve system performance and energy efficiency.

An adaptive user-application aware, learning-based embedded CPU power-saving approach was suggested by Lei Yang, Robert, et al. Many processor-intensive multimedia applications depend more on user and software than CPU use. Understanding may minimize CPU power. The suggested strategy saves electricity by forcing the CPU to adjust voltage and frequency for user performance. The proposed method was tested on Linux with the default ondemand governor.

V. CONCLUSION

Power management in embedded systems is the topic of this study. Discussed power management in embedded systems and discussed DVFS, Dynamic Power Management, architectural level, and application level approaches. Future embedded computer systems will need power-efficient audio, video, and connectivity. Power management in embedded systems must be assessed at all levels.

This paper aims to help researchers address power management challenges in embedded system design by suggesting that combining some techniques, such as hybrid techniques or improvements to the existing, may improve performance and power optimization. Developing energy-aware scheduling algorithms for modern multi-core embedded processors may also be a good idea.

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