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Adaptive Forward Body Bias Voltage Generator using 45NM Technology

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Abstract: *In both analog and digital circuits, the performance heavily relies on the threshold voltage (or turn-on voltage) of transistors. However, technology scaling doesn't proportionally reduce the threshold voltage relative to the aspect ratio of transistors. To tackle this challenge, the forward body bias (FBB) technique is employed to lower the threshold voltage of transistors. Thus enhancing device operating speed and enabling operation at lower supply voltages, albeit at the expense of forward biasing the bulk-drain or bulk-source junction. To overcome this challenge, an adaptive FBB voltage generator was designed to track the process and temperature variations by adjusting its output voltage accordingly. Notably, this adaptive FBB voltage also aids in reducing static leakage current through the bulk in comparison to a fixed FBB voltage. The proposed design has been simulated in 45nm Cadence Virtuoso, use of such newer technology nodes typically offers advantages over older nodes like 90nm in terms of performane, power efficiency, reliability and integration. When implemented in a 45nm technology node, the circuit retains its output without alteration, resulting in a reduced area, thereby providing an advantage in terms of area reduction. It is envisioned that integrating this solution into the digital signal processing (DSP) curriculum could elevate operating speeds and peripheral circuit performance of memory technologies such as SRAM, DRAM and others) thereby accelerating the read path and decreasing access time. Furthermore, analog circuits can leverage this solution to boost the transconductance of transistors by minimizing the threshold voltage*

Keywords: forward body bias, threshold voltage, adaptive FBB, fixed FBB, static leakage

I. INTRODUCTION

In recent times, miniaturisation influences the process variations on scaling technology yield has become notably pronounced, particularly at lower technology nodes. These variations can cause transistors to operate either slower or faster than the expected nominal behavior. Slower transistors can impede the overall circuit operating speed, while faster ones can lead to significantly higher leakage power consumption. To address these process variations, the Body Biasing technique is widely employed to adjust the threshold voltage of transistors, serving as a crucial aspect of performance and power management in modern System-on-Chips (SoCs).

Dynamically modulating bulk voltages and supply voltages (DVFS) in different operating modes of SoCs is key to achieving power savings and performance enhancements. Slower transistors' bulk terminals are FBB relative to the source or drain terminal to decrease their threshold voltage. While faster transistors' bulk terminals are Reverse Body Biased (RBB) relative to the source or drain terminal to increase their threshold voltage and reduce leakage power consumption. Besides global process variations, on-chip global variations also significantly impact yield at lower technology nodes.

Circuits that draw substantial current during operation dissipate power in the form of heat, which can locally raise the temperature within portions of the SoC. This temperature elevation reduces mobility, resulting in lower on-current and increased overall logic circuit delay. The resulting delay increase is due to local variations that can affect yield, but this can be mitigated by applying appropriate body bias voltage. Consequently, a literature survey is conducted regarding body-biasing generators in the subsequent section.

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II. THEORETICAL BACKGROUND

Crafting an adaptive forward bias voltage generator within a 45nm technology node using the Cadence tool demands meticulous attention in detail to achieve accuracy and efficacy. This generator plays a pivotal role in numerous analog and mixed-signal circuits, particularly in enhancing both performance and power efficiency

2.1 Circuit Description

The memory cell serves as a core circuit and comprises of following components:

1. Read/Write circuit
2. 6T SRAM(Static Random Acess Memory)
3. Sense Amplifier Circuit

The Bolck diagram of memory cell is as shown in Figure 1,

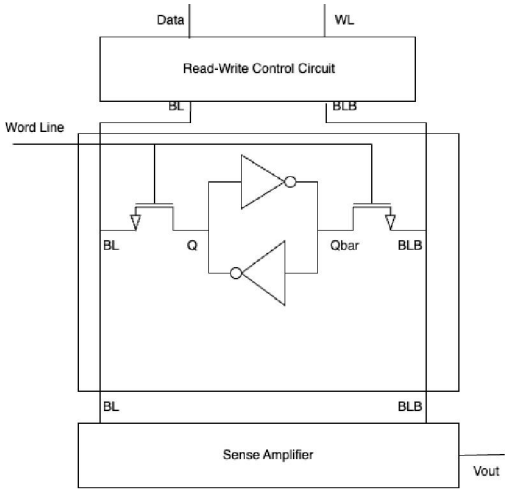

Figure 1: Block diagram of memory cell.

In Figure 2, the sense amplifier circuit of memory cell stands as a critical component in memory design. Its primary function is to monitor the bitline effectively, thereby enhancing the read and write speed of the memory cell while reducing power consumption. The sense amplifier achieves this by amplifying the voltage produced on the bitline during read/write operation. Given its pivotal role, the sense amplifier employs different circuits tailored for specific operations. Notably, in SRAM operations, where memory refresh is not required for further processing, still the sense amplifier operates non-destructively. During memory cell access, column multiplexers connect to the sense amplifiers, ensuring that each input corresponds to a single sense amplifier selection. This meticulous design enables optimal utilization of the sense amplifier within the circuit. Key parameters for evaluating the performance of a sense amplifier include gain (A = Vout/Vin) and sensitivity (S = Vinmin - least noticeable signal).

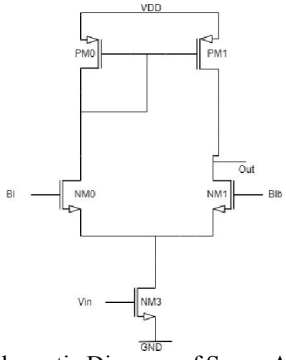

Figure 2: Schematic Diagram of Sense Amplifier circuit.

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Figure 3 shows read-write circuit of memory cell ,which is responsible for facilitating data read and write operations to and from the memory cell. This circuit comprises of essential components such as bitlines, write drivers, sense amplifiers, and control logic (e.g., write line). During a read operation, the control logic triggers the word line corresponding to the target memory cell, prompting the transmission of stored data onto the bitlines. The sense amplifier then plays a vital role by amplifying and comparing the voltage disparity between the bitlines to ascertain the stored data. In contrast, during a write operation, the control logic activates the wordline and applies the intended data to the bitlines using the write driver. Subsequently, the data stored in the memory cell is updated based on the voltage level present on the bitlines. The read-write circuit operates with high speed and low power consumption to ensure the efficient functioning of the SRAM. Notably, the sense amplifier and write driver consume the majority of power in the circuit, and their design prioritizes swift operation to minimize data access time.

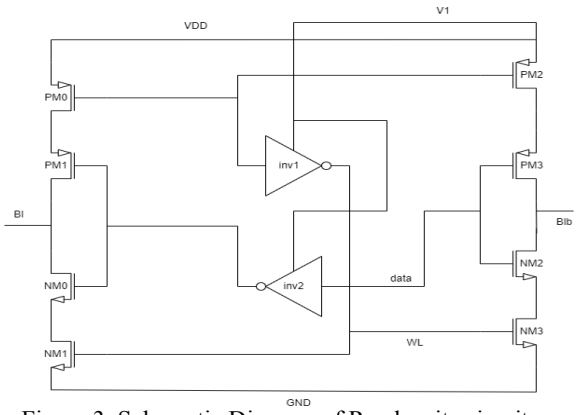

Figure 3: Schematic Diagram of Read-write circuit.

The SRAM cell of memory cell illustrated in Figure 4, utilizes six transistors for its functionality.

Write operation :

The Word Line(WL) is raised to a high voltage level, and the bit and bit bar lines are charged accordingly to the intended value. To write a logic 1, the bit line is charged to Vdd while the bit bar is maintained at 0. As the word line goes high, the access transistors close, writing the values to Q and Qbar, respectively. The process is reversed to write a logic 0.

Read operation :

The bit and bit bar lines are precharged to Vdd, and then the word line is activated. With the word line high, the bit and bit bar lines are left floating, and the access transistors close, allowing the values stored in the
cross-coupled inverters to transfer to the bit and bit bar lines. During the read, if Q is 1 and Qbar is 0, the bit line remains charged, retaining its value of 1, while the bit bar line discharges to ground, achieving a value of 0

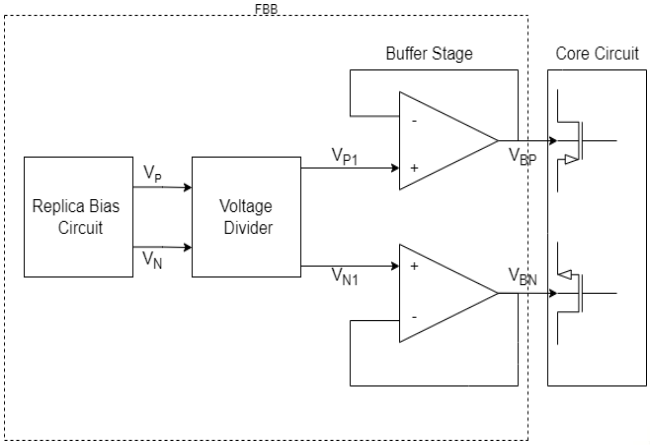

Figure 4: Schematic Diagram of 6T-SRAM circuit

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Hold operation

With the word line low, the access transistors(NM2, NM3) are open. As a result, there's no path for the values stored in the cross-coupled inverters to charge or discharge, ensuring that the values are maintained.

The design of conventional SRAM (Static Random Access Memory) requires a higher threshold voltage for its read and write operations. This higher threshold voltage can be a drawback when there is a need to reduce the power consumption of the overall circuit.

Implementing SRAM with adaptive body bias can help mitigate this issue by reducing the threshold voltage as needed. Adaptive body biasing involves dynamically adjusting the voltage applied to the body (or substrate) of the transistors in the SRAM cells. By doing so, it is possible to lower the threshold voltage during periods of operation that demand lower power consumption, thereby improving the overall energy efficiency of the circuit.

III. DESIGN AND IMPLEMENTATION

The implementation of an adaptive forward bias circuit involves several stages, including schematic design, simulation, layout, verification, and post-fabrication validation, all of which are facilitated using Cadence Virtuoso. Serving as a comprehensive platform, Cadence Virtuoso is utilized for designing and executing analog, mixed-signal, and custom digital integrated circuits. The process begins with the creation of circuit schematics using the Schematic Editor, followed by performance analysis conducted through Spectre simulations. Subsequently, designers transition to the Layout Editor to generate physical representations of the circuit, verifying their designs using tools like Assura or Calibre. This thorough workflow encompasses crucial verification steps such as Design Rule Checking (DRC) and Layout vs. Schematic (LVS), ensuring consistency between the schematic representation and the physical layout of the circuit.

A. Block Diagram

Figure 5 shows the block diagram of Adaptive body-biased circuit. The proposed circuit relies on a replica biased circuit composed of forward-biased internal diodes of NMOS and PMOS, respectively. The outputs of this replica biased circuit, VP and VN, can be further adjusted using a voltage divider circuit to configure the body bias voltage for various modes of operation of the SoC. The output of the divider is then passed through a voltage buffer or regulator stage. It is essential to design the voltage buffers to accommodate the maximum current and capacitive load of the target application. The output voltage of FBB for PMOS(V_{BP}) acts as a current sink because the leakage current is injected into it. Conversely, for NMOS(V_{BN}) acts as a current source because leakage current is drawn from it.

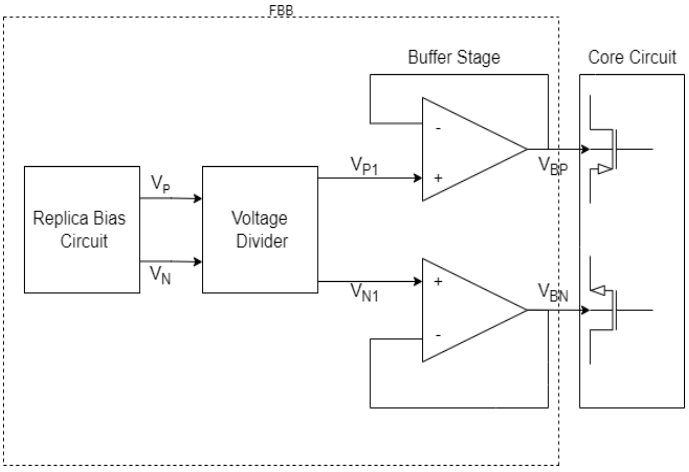

Figure 5: Block diagram of adaptive body bias generator.

The replica bias circuit, as implemented in Cadence Virtuoso, is depicted in both Figure 6 and Figure 7.

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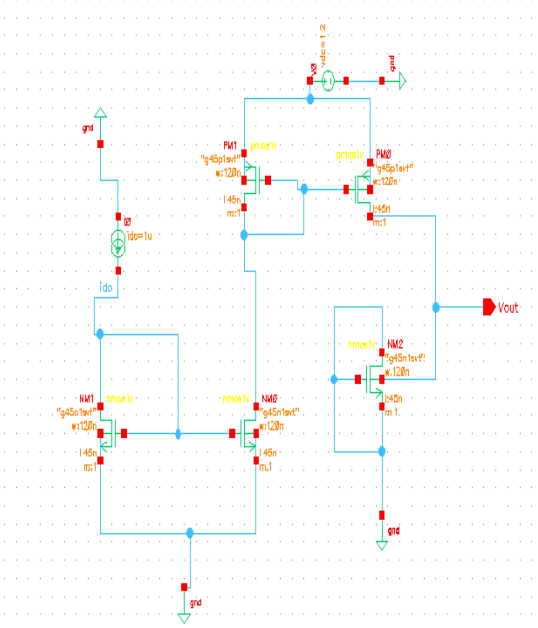


Figure 6: Forward baising of intrinsic diodes of NMOS transistors

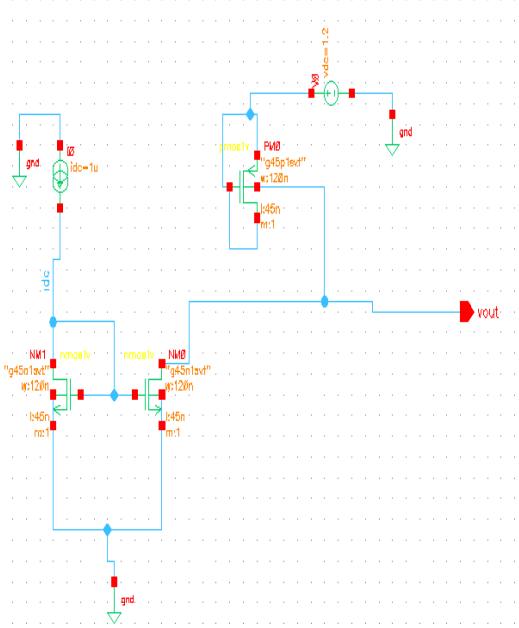
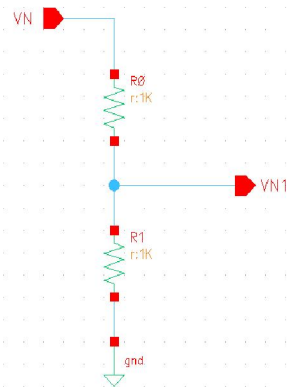


Figure 7: Forward baising of intrinsic diodes of PMOS transistors

In Figure 8 and 9, a voltage divider circuit for NMOS and PMOS is depicted, using two series resistors and an input voltage.



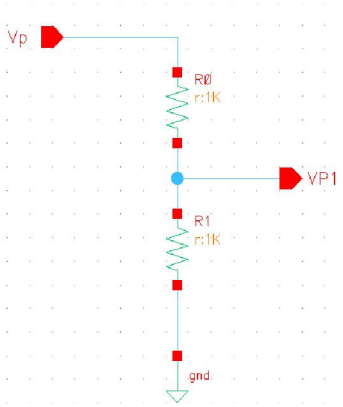


Figure 8: Voltage divider of NMOS circuit Figure 9: Voltage divider of PMOS circuit

Figure 10 shows the circuit diagram of the FBB Voltage Regulator for PMOS, using a two-stage unity gain buffer. Within this setup, an error amplifier (EA) is employed to regulate the gate voltage of the final stage NMOS transistor (Mno of Figure 5). The choice of the final PMOS stage for the NMOS FBB Generator is based on its capability to provide a load current in the form of leakage current. Conversely, the final NMOS stage is selected for the PMOS FBB generator since it is designed to handle sinking current loads. This circuit is constructed using a two-stage differential pair comprising transistors M0-M4 and M5-M8. The biasing voltage Vbias is utilized to bias the initial current transistors M2 and M9. To ensure stability against maximum capacitive and current loads, the buffer is equipped with a miller capacitance (Cm) and zero nulling resistance (Rz). The bias voltage VB is applied to bias the transistors M2 and M9

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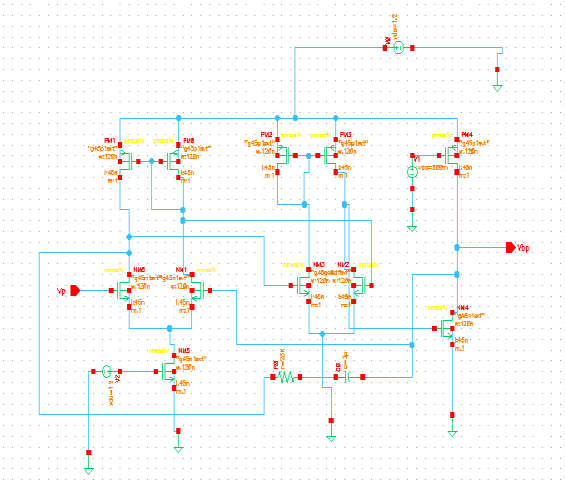

Figure 10: Schematic Diagram of unity gain buffer of PMOS transistors

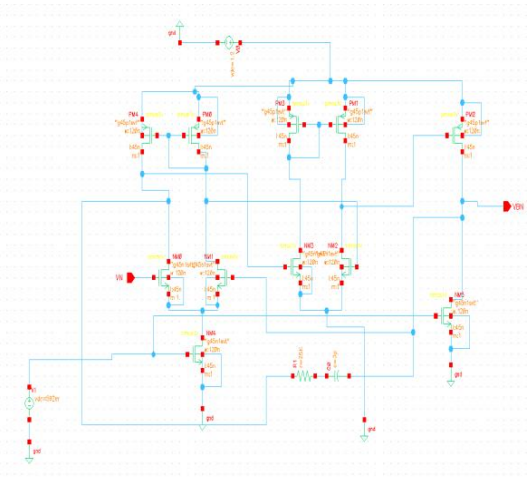

Figure 11: Schematic Diagram of unity gain buffer of NMOS transistors

Similarly, Figure 11 illustrates the transistor-level implementation of a unity gain buffer for the FBB generator designed for NMOS. The design of the buffers aims to establish their internal pole dominance at node V1. However, in scenarios where there is a need of drive exceptionally large load capacitance, adjustments can be made to prioritize the pole arising from the load capacitance as dominant.

Figure 12 illustrates the schematic implementation of a memory cell utilizing reduced threshold voltage without applying Adaptive Forward Body Bias in 45nm CMOS technology.

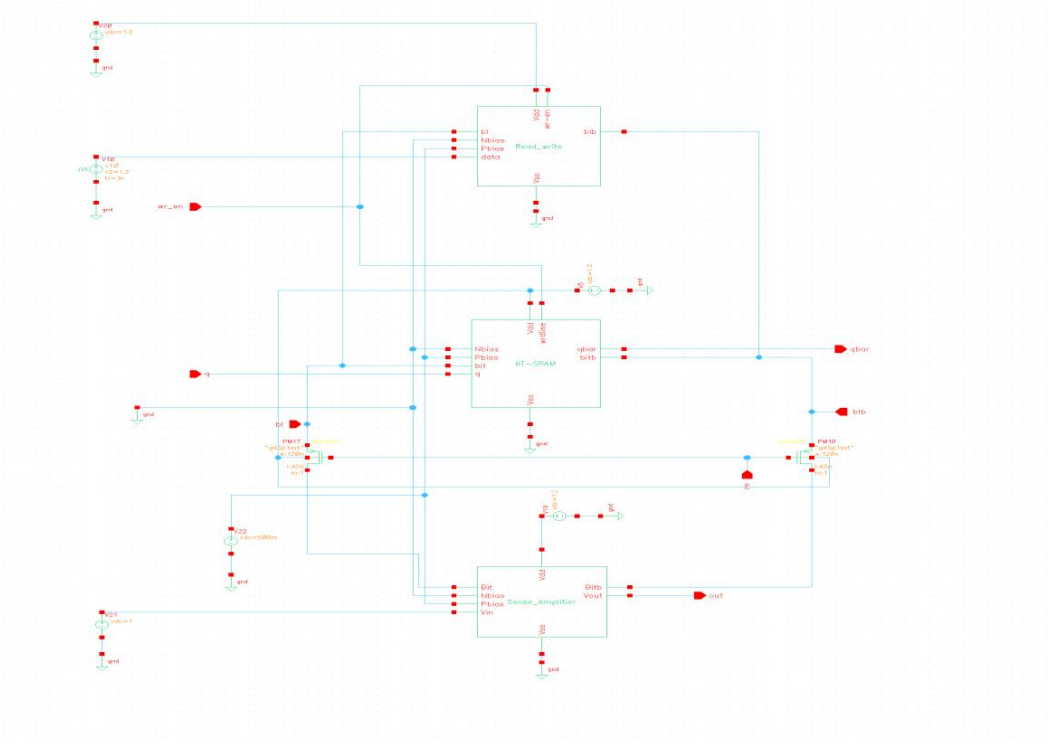

Figure 12: Schematic implementation of SRAM cell Without Adaptive Forward Body Bias

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Figure 13 illustrates the schematic implementation of a memory cell utilizing reduced threshold voltage by applying Adaptive Forward Body Bias in 45nm CMOS technology

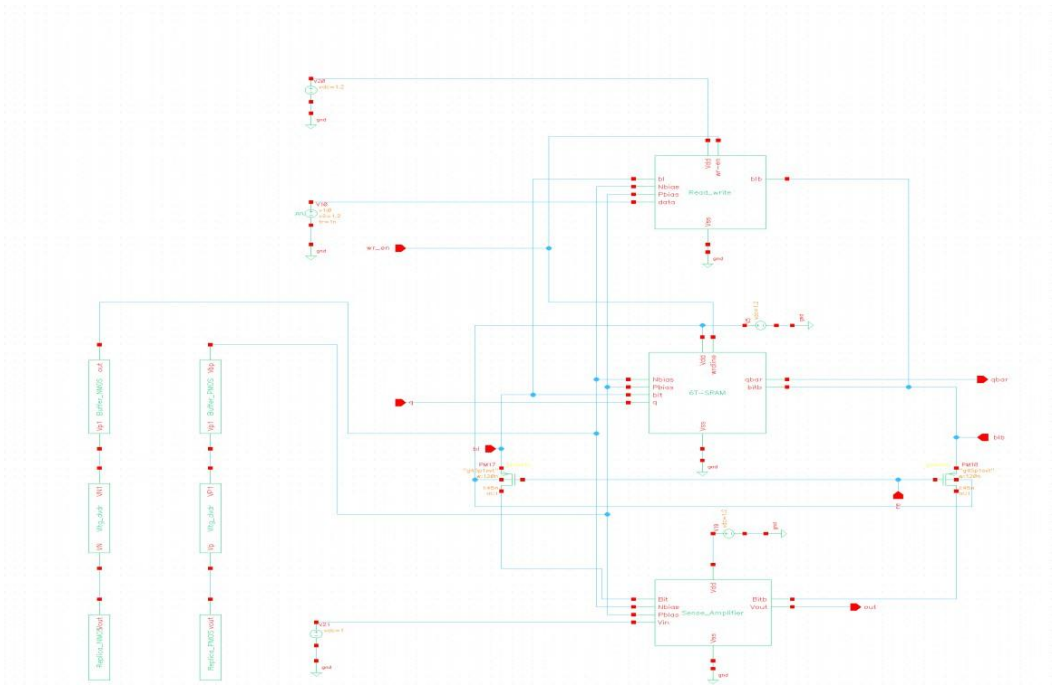
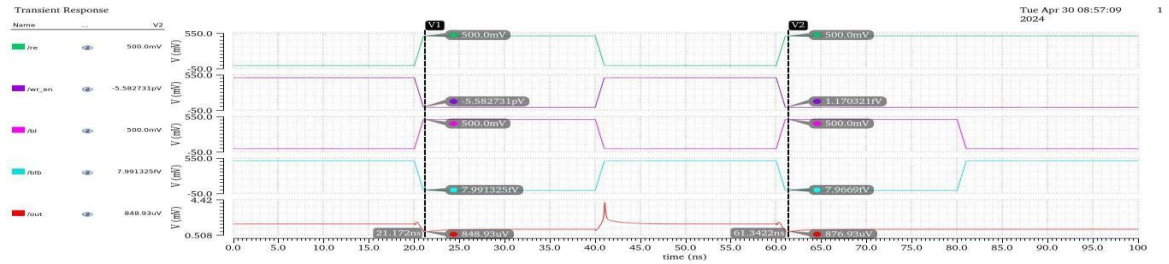


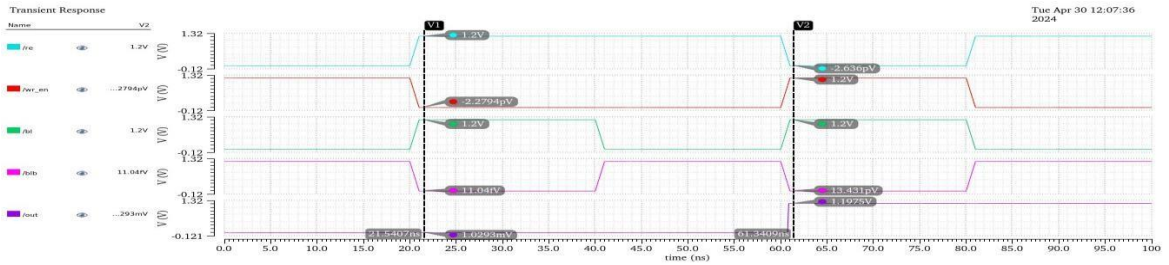
Figure 13: Schematic implementation of memory cell with Adaptive Forward Body Bias

IV. RESULTS AND DISCUSSIONS

The comparison of the output waveforms of a memory cells which contain two graphs without adaptive body bias when given threshold voltages of 500mV and 1.2V as shown in Figure 14(a) and Figure 14(b) respectively. Both graphs indicate voltage levels for read, write, bl, blb, and output sequentially.



(a)



(b)

Figure 14: Output waveform of Memory Cell With threshold voltage, (a) 0.5V (b) 1.2V.

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This comparison discusses the effect of threshold voltage and adaptive body bias on the performance of a memory cell.

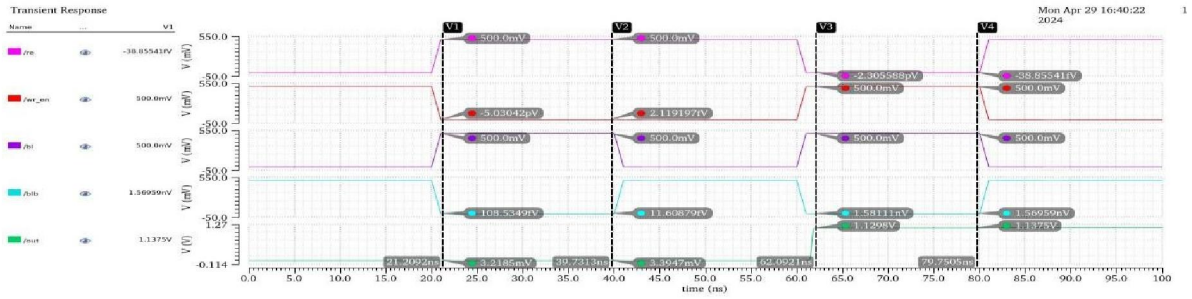
Initially, the performance of the memory cell is assessed with different threshold voltage settings. At a threshold voltage of 500mV, the output is indistinct, indicating that the memory cell does not operate effectively under these conditions. This could mean that the signal is too weak or noisy to be reliably interpreted, leading to potential errors or instability in memory operation.

When the threshold voltage is increased to 1.2V, the output becomes distinct. This suggests that the memory cell requires a higher threshold voltage to function correctly, providing a clearer and more reliable signal. The higher voltage likely enhances the driving strength of the transistors within the memory cell, improving its overall performance and stability.

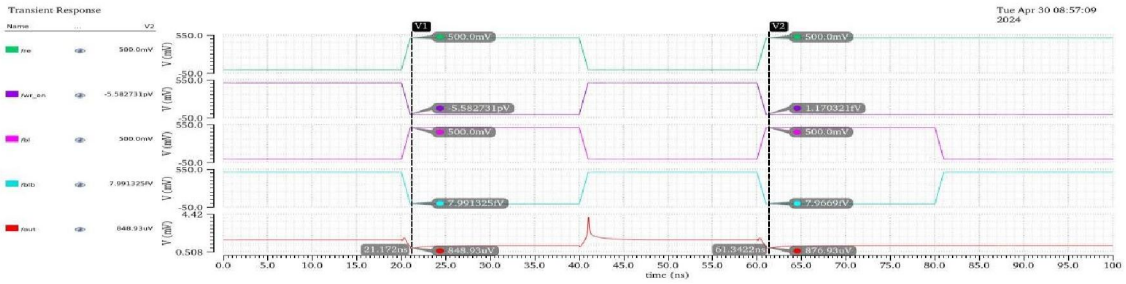
Adaptive body bias is a technique used to adjust the threshold voltage of a transistor dynamically by applying a bias voltage to its body terminal. When adaptive body bias is applied to the memory cell, it allows the cell to operate effectively even at the lower threshold voltage of 500mV. This means that the threshold voltage requirement for distinct output is reduced due to the adaptive body bias technique.

Thus, the application of adaptive body bias demonstrates a significant improvement in the performance and versatility of the memory cell, enabling effective operation at lower threshold voltages that were previously insufficient for distinct output.

The comparision of output waveforms as shown in Figure 15(a) and Figure 15(b) contain two graphs showing memory cells with and without ABBF. Both graphs indicate voltage levels for read, write, bl, blb, and output sequentially.



(a)



(b)

Figure 15: Output waveform of memory cell, (a) with Adaptive FBB (b) without Adaptive FBB.

In an analysis of the performance characteristics of memory cells, a comparison was made between cells utilizing adaptive body bias (ABB) and those without it. The findings revealed that memory cells equipped with ABB exhibited significantly better performance, delivering output waveforms that aligned precisely with the desired specifications. This indicates that the adaptive body bias mechanism effectively enhanced the functionality of these cells.

On the other hand, memory cells that did not employ adaptive body bias showed degraded performance. Despite having the same threshold voltage of 500mV, these cells produced corrupted output waveforms. This discrepancy highlights the critical role of adaptive body bias in maintaining the integrity and reliability of memory cell operations. The

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adaptive body bias technique dynamically adjusts the body voltage of the transistor, which can mitigate variations and improve the overall performance. This dynamic adjustment allows the memory cell to respond better to different operating conditions and variations in the manufacturing process, ensuring stable and accurate output waveforms

In contrast, memory cells without ABB lack this adaptive capability, leading to poorer performance and unreliable output, as they are more susceptible to variations and unable to dynamically correct their threshold voltage during operation. This ultimately results in corrupted output waveforms, emphasizing the importance of implementing adaptive body bias in memory cell designs for optimal performance.

V. CONCLUSIONS

The output magnitude of FBB generator is dependent on fixed current that is used to bias the intrinsic p-n junction formed in NMOS and PMOS. It also limits the leakage current consumption and keeps the leakage current load due to forward biasing of n-well and p-well, fixed across temperature and process variations. The applications of ABB generator can be applied to emerging memories and timing critical paths to gain the performance without having significant area overhead. The findings obtained underscore the critical role of adaptive body biasing in enhancing the reliability and robustness of memory cell operation, particularly in ensuring the faithful reproduction of desired output signals. The future scope of adaptive forward body bias voltage generators lies in their potential to optimize energy efficiency and performance in advanced semiconductor technologies, especially in low-power and high- performance applications like IoT devices, wearables, and mobile computing. As chip designs continue to shrink and power constraints become more critical, adaptive forward body bias voltage generators can play a crucial role in dynamically adjusting power consumption while maintaining performance levels, enhancing battery life, and extending device longevity.

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