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# Design and Implementation of Low Power Comparator Based Flash ADC

**M. Kusuma Sri, J. Aparna Priya, B. Hemalatha, Amrita. S**
Anurag University, Hyderabad, India

**Abstract:** *This project describes the design of a high-speed latched comparator with a 6- bit resolution, full-scale voltage of 1.6 V, and a sampling frequency of 250 MHz. The comparator is designed in a 0.35 µm CMOS process with a supply voltage of 3.3 V. The comparator is designed for time-interleaved band-pass sigma-delta ADC. Due to the nature of the target application, it should be possible to turn off the components to avoid static power consumption. The comparator of this design implements the turn-off technique when it is not in use. The settling time of thecomparator is less than half the clock cycle which means it does not affect the functionality of the band-pass sigma-delta ADC in terms of speed. The simulation results are derived using Cadence environment. The results show that the comparator has 6-bit resolution and power consumption of 4.13 mw for the worst-case frequency of 250 MHz. It fulfills all the performance requirements, most of them with large margins.*

**Keywords:** ADC

## I. INTRODUCTION

ADC stands for Analog-to-Digital Converter. It's a crucial component in electronics that converts continuous analog signals into discrete digital representations. In simpler terms, it takes real-world signals like sound, light, temperature, etc., and turns them into digital data that a computer or digital system can process.

ADCs works by following steps:

- Sampling: ADCs sample the input analog signal at regular intervals. This means they take snapshots of the analog signal's value at specific points in time.
- Quantization: Once sampled, the analog signal's amplitude needs to be quantized,i.e., represented by a finite set of digital values. This process involves dividing therange of analog values into a finite number of intervals and assigning a digital codeto each interval.
- Encoding: The quantized analog values are then encoded into digital representations, typically in binary format. The number of bits used for encoding determines the resolution of the ADC. Higher resolution means more bits and thusmore precise representation of the analog signal.
- Conversion: Finally, the encoded digital values are transmitted or stored for further processing by digital systems, such as microcontrollers, DSPs (Digital Signal Processors), or computers.
- Parallel Architecture: In a Flash ADC, each bit of the digital output is generated in parallel. This means that the converter employs 2^n - 1 comparators for an n-bit conversion, making it very fast but also more complex and power-hungry compared to other ADC architectures.
- Comparators: The heart of a Flash ADC is its array of comparators. Each comparator compares the input analog voltage against a different reference voltage.
- Encoding: Based on the comparator outputs, a priority encoder determines the digital output. The encoder selects the highest-order active comparator and generates a binary output corresponding to its position.

**Characteristics:**

- Speed: Flash ADCs are among the fastest ADCs available, capable of samplingrates in the gigahertz range.
- Power Consumption: Flash ADCs consume more power compared to other ADCarchitectures due to their large number of comparators operating in parallel.

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- Area: The area required for a Flash ADC is relatively large, especially for higher resolutions, because of the need for multiple comparators.
- Parallelism: The parallel architecture allows for simultaneous conversion of all bits, eliminating the need for a conversion cycle.
- Linearity**:** Flash ADCs offer excellent linearity due to their simple architecture and lack of conversion errors like those found in successive approximation or pipeline ADCs.

The scope of this work is the design of a comparator for a time-interleaved bandpass Sigma-Delta ADC. The design is implemented in a 0.35 µm technology with 6 bits of resolution at a sampling frequency of 250 MHz. The main consideration is to minimize the power consumption and avoid static power consumption by switching it off when it is not in use.

## II. LITERATURE REVIEW

Glyny George, A. V. Jos Prakash, "Design of ultra-low voltage high-speed flash ADC in 45nm CMOS Technology", IEEE Conference on recent trends in electronics, Information & Communication Technology, 2019.

The paper by Glyny George and A. V. Jos Prakash presents the design of an ultra- low-voltage high-speed Flash ADC implemented in 45nm CMOS technology. The aim is to achieve both low-voltage operation and high-speed performance. The authors discuss the challenges associated with low-voltage operation and propose innovative design techniques to address them. They detail the architecture of the Flash ADC, highlighting key features such as the comparator design, reference voltage generation, and error correction mechanisms.

The design is optimized for high-speed operation while maintaining low power consumption. Simulation results demonstrate the effectiveness of the proposed approach in achieving the desired performance metrics. Overall, the paper contributes to advancing the state-of-the-art in Flash ADC design for low-voltage applications.

Mirza Nemath Ali Baig, Rakesh Ranjan, " Design and implementation of 3-bit High-speed flash ADC for wireless LAN Applications", IJARCCE, Vol 6, 2020.

The paper authored by Mirza Nemath Ali Baig and Rakesh Ranjan presents the design and implementation of a 3-bit high-speed Flash ADC tailored for wireless LAN applications. The focus is on achieving fast conversion speeds to meet the requirements of wireless communication systems. The authors discuss the specific challenges and constraints posed by wireless LAN applications, such as the need for high throughput and low power consumption. They detail the architecture of the Flash ADC, including the comparator design, reference voltage generation, and digital logic for encoding the output. The design is optimized for high-speed operation while ensuring accuracy and reliability.

Experimental results validate the performance of the ADC in meeting the requirements of wireless LAN applications, showcasing its suitability for integration into communication systems. Overall, the paper contributes to advancing the field of ADC design for wireless communication applications.

Al-Ahsan Talukder, Md. Shamim Sarker, "A three-bit threshold inverter quantization based CMOS flash ADC", 2019 4th International Conference on Advances in Electrical Engineering, 2019

The paper was authored by Al-Ahsan Talukder and Md. Shamim Sarker presents a novel approach to Flash ADC design using a three-bit threshold inverter quantization technique. The focus is on improving the efficiency and speed of the ADC while maintaining accuracy. The authors discuss the implementation of the threshold inverter quantization method in CMOS technology, detailing its advantages over traditional Flash ADC architectures. They describe the operation of the proposed ADC architecture, including the threshold inverter quantization process and the encoding scheme for digital output. Simulation results demonstrate the effectiveness of the approach in achieving high-speed conversion with reduced power consumption.

Sonu Kumar, Anjali Sharma, "Design of CMOS operational amplifier in 180nm technology",
International Journal of Innovative Research in Computer and Communication Engineering Vol.5, issue 4, April 2017.

The paper authored by Sonu Kumar and Anjali Sharma focuses on the design of a CMOS operational amplifier (op-amp) in 180nm technology. The objective is to develop an operational amplifier with high-performance characteristics suitable for modern integrated circuits. The authors discuss the design considerations, such as gain, bandwidth, and stability, specific to CMOS technology in the 180nm process node. They detail the circuit topology and architecture chosen for the operational amplifier design, including transistor sizing and biasing schemes. Simulation results

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demonstrate the performance metrics achieved by the proposed op-amp design, such as gain-bandwidth product, slew rate, and power consumption.

M.P. Ajanya, George Tom, "Low power Wallace tree encoder for flash ADC",IOP conference series: Material science and engineering 2018.

The paper authored by M.P. Ajanya and George Tom presents a low-power Wallacetree encoder designed specifically for Flash ADCs. The focus is on reducing power consumption while maintaining high-speed operation, a crucial aspect in modern ADC designs. The authors discuss the challenges associated with power efficiency in ADC encoders and propose the utilization of the Wallace tree encoding techniqueto address these challenges. They detail the architecture and implementation of the low-power Wallace tree encoder, highlighting the advantages it offers in terms of reduced power consumption and improved efficiency. Experimental results presented in the paper validate the effectiveness of the proposed approach in achieving low-power operation without compromising the performance of the FlashADC.

## III. METHODOLOGY

In Existing method, Flash Analog to digital converter is implemented whose resolution is 3-bits. The designed Flash ADC consists of a resistive ladder network, comparators, the thermometer to a binary encoder and the entire design is carried out using LTspice tools employing 180nm technology. The reference voltage applied to the resistive ladder network is 1.8V. A two-stage operational amplifier is used as a comparator in the flash ADC. Binary code is obtained from the thermometer code byutilizing a priority encoder.

The major problem that usually appears in flash ADC is as the number of resolutionbits increases, the Area, as well as the power consumption of the circuit, also increases. In this paper, we principally concentrated to lessen the power consumptionof the ADC by optimizing encoder circuitry. With the purpose of reducing power consumption, Encoder is implemented using 2:1 mux based on various logics such as switch logic, pass transistor logic as well as CMOS logic.

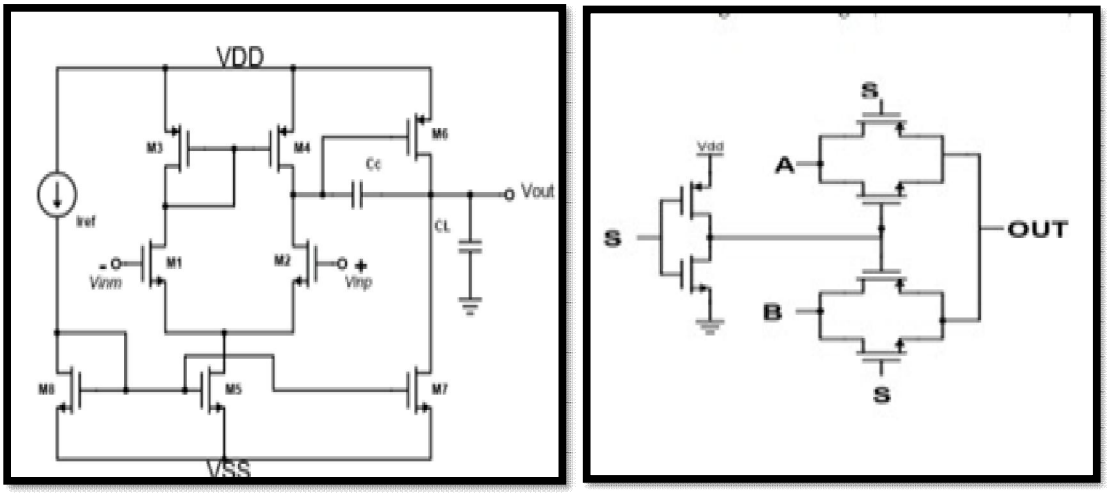


**Figure 1.** Flash Adc implemented using 2x1 mux CMOS switching logic and op-amp

In Existing design, we have implemented flash ADC with a 3-bit resolution. Designand simulation of 3-bit flash ADC are carried out using the LTspice tool employing180nm technology model files. Parameters such as conversion time, the average power of 3-bit flash ADC are calculated and compared. Mainly we focused to reducethe power consumption of 3-bit flash Adc by optimizing the encoder circuitry.

The encoder is implemented using different design styles such as Wallace tree encoder, 2:1 mux based encoder. It is verified that 3 bit Flash ADC designed utilizinga Wallace tree encoder offers less power compared to a 2:1 mux based encoder. Also,we have implemented a 2:1 mux based encoder employing different design logics such as switch logic, pass transistor logic, and complementary metal- oxide semiconductor logic. out of these logics, 3-bit Flash ADC implemented utilizing encoder with CMOS 2:1 mux consumes less power and offers less delay. Further, it is intended to increase the resolution of flash ADC and also to reduce theaverage power consumed by the circuit by optimizing the flash ADC circuitry.

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Digital signal processing has advanced intensely due to the rapid expansion of science and technology. In the majority of the digital domains, signal processing offers several advantages such as flexibility in design and programmability, reduced silicon area, high accuracy, as well as a smaller amount of power consumption. The design process is cost-effective and faster. Hence it is possible to design a system with a lesser area along with high speed. It is required to have an analog to digital converter that offers much higher speed in wireless communication, image processing, etc[1].

It is preferred to have digital systems that are portable and have prolonged battery life. This can be only possible by developing applications that consume less power. Since ADC's act as front-end components in the majority of mixed-signal systems, we focused to design ADC that consumes less power which in turn offers higher speed. We have various types of ADC architectures for instance successive approximation type ADC, Flash type, sigma-delta, etc.

Among these Flash ADC is preferred since it offers high speed because of its parallelarchitecture, the conversion time is not limited by resolution hence these ADC's areutilized in those systems where bandwidth with a wide range and high speed is required[2]. Al-Ahsan Talukder and Shamim Sarker have implemented flash ADC with 3-bit employing threshold inverter quantization(TIQ). The main feature of this technique is the absence of separate reference voltage power supplies, unlike other Flash ADC implementations. It is possible to set the switching voltage of the inverter by choosing nmos as well as pmos transistors with suitable width to length ratios.

This architecture comprises of TIQ comparator, the thermometer to the binary encoder in addition to gain booster. Because of the change in the dimensions of comparator Area changes [3]. Sonu Kumar and Anjali Sharma proposed a strategy employing CMOS technology that is demonstrated for implementing opamp. They preferred CMOS technology for designing an operational amplifier due to the fact that CMOS devices consume low static power and these devices are highly withstanding noise.

The two-stage operational amplifier performance parameters are obtained whose gain is 44.98dB, the phase margin is 63 degrees, the gain-bandwidth product is 33.4MHz, power consumption 276µW[4].Mirza Nemeth Ali Baig and Rakesh Ranjan have implemented high-speed flash ADC for wireless LAN applications. The designed 3-bit flash ADC is implemented using seven operational transconductance based comparators with the reference voltage of 250mV and a high-speed encoder is implemented using full adders. This design is a flash-based ADC converter with a finite output resolution of three bits and power consumption of about 223µW and resides in a chip area of 0.089287 mm2. The high-speed flash ADC is being designed and verified using the CADENCE Virtuoso tool with CMOS 180 nm technology. Since ADC is implemented by utilizing a full adder based encoder, The area is limited by the resolution[5].

## IV. RESULTS AND DISCUSSION

The latched comparator design has been simulated using Cadence tools for different parameter values. The full-scale voltage of the comparator is 1.6 V (0.4 V to 2.0 V). The comparator was optimized for the sampling frequency of 250 MHz. The comparator works up to the maximum frequency of 300 MHz for 6-bit resolutions. Figure 2 gives the pictorial explanation of comparator inputs. The output values are calculated by applying the ramp signal at the input of the comparator and a referencedc signal.

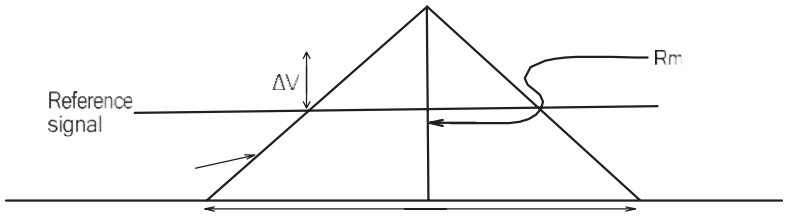


**Figure 2.** Comparator inputs model

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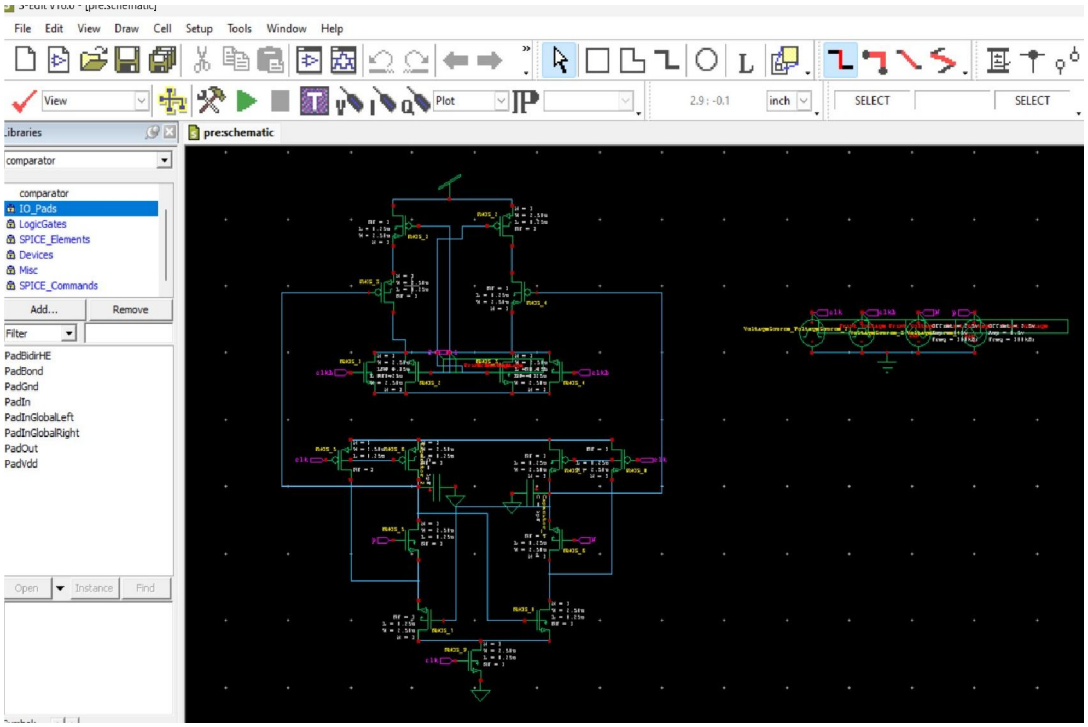


**Figure 3.** schematic design of the flash Adc implantation using Comparartor

The design has been simulated for different frequencies and reference values. The following table shows the results when a ramp signal is applied as an input.

**Table 1.: Simulation results when a ramp signal is applied as an input**

| No. | Frequencies (MHz) | Ramp signal(v) | Ref.(v) | simulationtime (us) | V (mv) | Res. (N) |
|---|---|---|---|---|---|---|
| 1 | 250 | 0.5 - 0.7 | 0.6 | 3.0 | 9.01 | 7.5 |
| 2 | 250 | 1.1 -1.3 | 1.2 | 3.0 | 1.56 | 9.96 |
| 3 | 250 | 1.8 - 2.0 | 1.9 | 3.0 | 0.596 | 11.39 |
| 4 | 300 | 0.5 - 0.7 | 0.6 | 3.0 | 24.1 | 6.059 |
| 5 | 300 | 1.1 - 1.3 | 1.2 | 3.0 | 13.05 | 6.943 |
| 6 | 300 | 1.8 - 2.0 | 1.9 | 3.0 | 19.55 | 6.35 |

The simulation time has been calculated for different frequencies and the ramp signal of 0.2 V. The resolution (Rm) used for measurements is 0.1 mV. All the simulation values for this thesis work are derived using the Tanner

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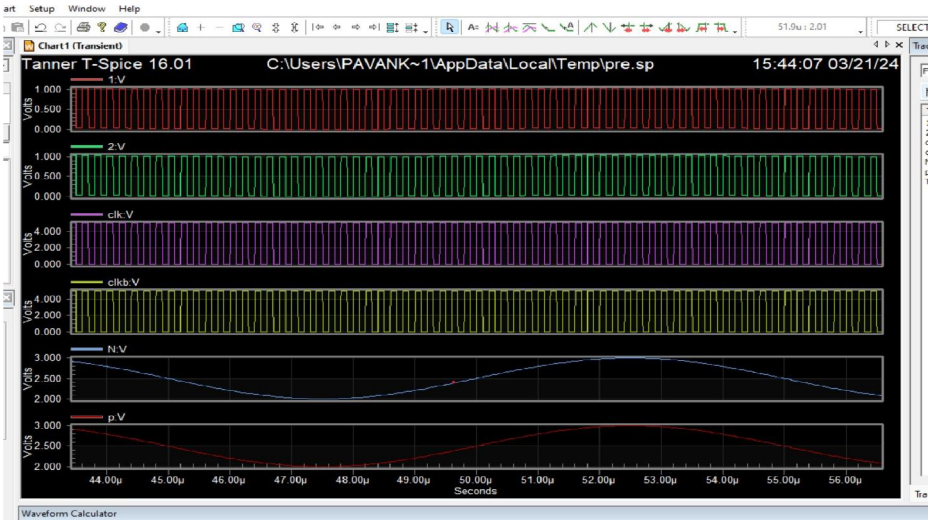


**Figure 4.** Simulation Waveforms for designed Flash ADC using Comparator

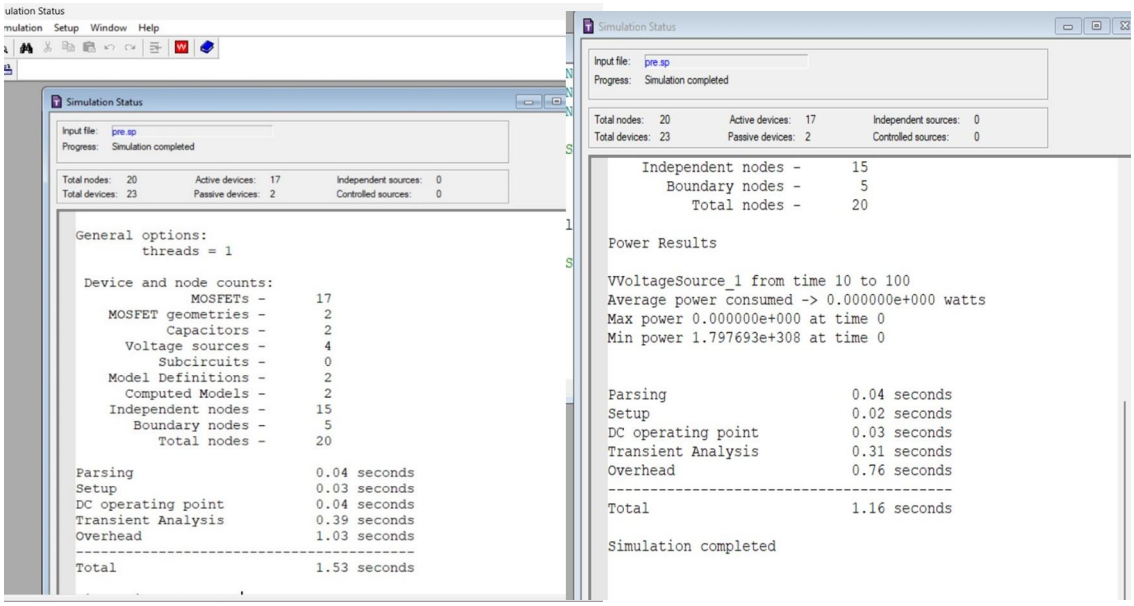


**Figure 5.** Area and Delay calculations of the schematic design

The performance and design parameters of the latched comparator are presented in Table 4.1. The values are taking by applying the non ideal inputs with load resistanceof 300 Ω and 1.5 fF capacitance.

Table 2. Design parameters Simulation results of the comparator

| | |
|---|---|
| Power consumption | 4.136 mW |
| Comparator Gain | 5.876 |
| -3dB cutoff frequency | 730.93 MHz |
| Unity gain frequency | 1.021 GHz |
| Input DC voltage | 1.65 V |
| Comparator Biasing current | 201.2 µA |
| Static power consumption | 81.08 pW |
| Kickback suppression | 12.2 dB |

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Table 2 shows several parameters such as power consumption, comparator gain, and static power consumption. The power consumption was calculated both when the comparator was "ON" and "OFF" with a sampling frequency of 250 MHz and 3.3 V power supply.

## V. CONCLUSION

The purpose of this project work was to design a latched comparator for time- interleaved bandpass sigma-delta ADC with 6-bit resolution, the sampling frequency of 250 MHz, and full scale voltage of 1.5 V using 0.35 µm process with a supply voltage of 3.3 V. The simulation results in Table 4.1 show that the comparator fulfills the requirements.

The most difficult part in this design was the optimization of NMOS and PMOS for proper operation and also the comparator turn-off technique when it is not in use to avoid static power consumption. However after careful analysis of the simulation and design at different points the goal was achieved. Also, the comparator was successfully turned off with almost zero static power consumption. The comparator fulfills all the other requirements with a good margin and has been simulated for worst cases. It can work up to the sampling frequency of 300 MHz. The reference signal was compared with a ramp input signal at ±0.1 V level from lower and upper boundary with satisfactory results.

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