IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
Volume 7, Issue 2, July 2021
Impact Factor: 4.819

Implementation of Fir Filter Using Distributed Arithmetic and Distributed Arithmetic Off-Set Binary Coding Algorithms

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Abstract: *This paper is the study of implementation of FIR filter using Distributed Arithmetic and Distributed Arithmetic Offset Binary Coding Algorithms. Distributed Arithmetic (DA) had been used to implement an FIR filter due to its high stability and linearity by using look-up table (LUT). The performance of DA technique and DA-OBC for FIR filter design is analyzed and the results are compared to the traditional FIR filter design techniques.*

Keywords: DA, DA-OBC

I. INTRODUCTION

In signal processing, a finite impulse response filter is a filter whose impulse response is of finite duration, because it settles to zero in finite time. Nowadays Finite impulse response filters have got huge importance in fields like digital signal processing, wireless communication and also in the fields where the complexity is less. People are expecting a system which have good accuracy, efficiency and error-free in their operation. In the field of Digital signal processing, an FIR filters are used to implement any sort of frequency response digitally. It has a number of useful properties compared to an IIR, i.e., inherently stable, no feedback required and designed to be in linear phase. The core of the FIR filter implementation is multiplication and accumulation (MAC) operation. The design method of MAC can be defined using various algorithm and techniques. Distributed Arithmetic (DA), it is a computational algorithm that performs multiplication with look up table based schemes. The derivation of this algorithm is extremely simple. DA-Offset Binary Coding (DA-OBC) based architecture, will decrease the LUT size by half and make operation speed faster.

II. LITERATURE SURVEY

Sumbal Zahoor, Shahzad Naseem, Wei Meng (Reviewing editor) on 07,Aug,2017 proposes a novel method for Design and Implementation of an Efficient FIR digital filters. In this paper the design methods of FIR filters is discussed by employing various window functions. The band pass filter of order 38 and 48 is observed one by one and analyzed that Kaiser window gives better results [1].

S. R. Reddy, P. Jayakrishnan in April 2017 made an effort to explain the Design of FIR filter based on Improved DA and Implementation to High Speed Ground Penetrating Radar System. This paper proposes an improved distributed algorithm (DA) to implement high order digital FIR filters with less logical delay and hardware utilization. Firstly, the parallel DA is designed and then improved by look-up-table (LUT) decomposition. Secondly, the improved DA FIR filters are implemented on the Xilinx kintex-7. FPGA chip and used in high speed ground penetrating radar (GPR) system to process radar signals[2].

Implementation of FIR filters on FPGA using DA-OBC algorithm is proposed by Bo hong in which he conveys digital filters are basic units in many digital signal processing system. They have wide applications in communication, image processing and pattern recognition.

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The realization of FIR filters using hardware implementation uses the chip such as FPGA. It adopt the kaiser window to design. Its unit sampling h(n) is calculated on MATLAB software[3]. Qi Yue et al in 2005 proposed an idea of Lowpower FIR filter based on standard cell. This paper compares three low power schemes for the multi-hierarchy pipeline design of fixed point finite impulse response (FIR) digital filters, and we adopt an optimal CSD encoding method, minimizing the number of adders/subtractions in the design. In addition, a 16-bit, 16 taps low-pass FIR filter is designed to investigate the performance of the three different algorithms.[4] Kumari K Dhobi, Dr. K R Bhatt, Dr. Y B Shukla in March 2014 proposed FPGA Implementation of FIR Filter using Various Algorithms: A Retrospective which says that DA structure is easy to implement on FPGA because of pre-calculated results are already stored in LTUs and in FPGA it is easy to design. FPGA is an alternative solution for realization of digital signal processing filter. According to simulation result, Kaiser window method is the best window method[5].

III. METHODOLOGY

3.1 Distributed Arithmetic Algorithm

Distributed Arithmetic is a computation algorithm, which converts calculation of MAC to a serial of look up table accesses and summation. It was initially proposed by Croisier in 1973 and further developed by Peled and Lui. The principle of DA algorithm is as follows:

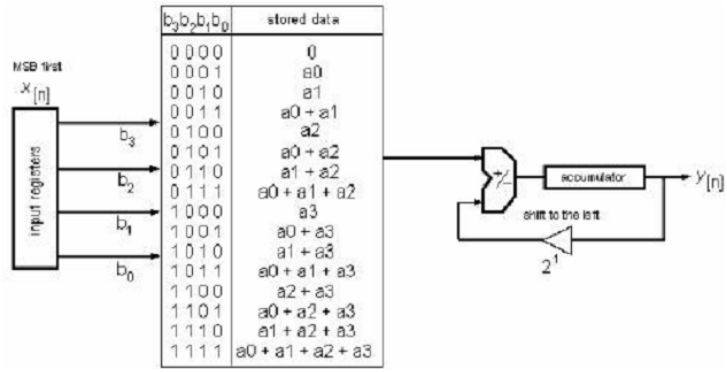
An FIR filter of N order is shown below

$$y(n) = \sum_{k=0}^{N-1} h_k x_k(n)$$

where y(n) is the output data, k(n) is the input data it can be expressed as

$$x_k = -x_{k,m-1} + \sum_{j=1}^{m-1} x_{k,m-1-j} 2^{-j}$$

Block diagram:



$b_3b_2b_1b_0$	stored data
0 0 0 0	0
0 0 0 1	a0
0 0 1 0	a1
0 0 1 1	a0 + a1
0 1 0 0	a2
0 1 0 1	a0 + a2
0 1 1 0	a1 + a2
0 1 1 1	a0 + a1 + a2
1 0 0 0	a3
1 0 0 1	a0 + a3
1 0 1 0	a1 + a3
1 0 1 1	a0 + a1 + a3
1 1 0 0	a2 + a3
1 1 0 1	a0 + a2 + a3
1 1 1 0	a1 + a2 + a3
1 1 1 1	a0 + a1 + a2 + a3

LUT Table:

The contents of look up table are constructed and stored before the execution.

$b_3b_2b_1b_0$	stored data
0 0 0 0	0
0 0 0 1	a0
0 0 1 0	a1
0 0 1 1	a0 + a1
0 1 0 0	a2
0 1 0 1	a0 + a2
0 1 1 0	a1 + a2
0 1 1 1	a0 + a1 + a2
1 0 0 0	a3
1 0 0 1	a0 + a3
1 0 1 0	a1 + a3
1 0 1 1	a0 + a1 + a3
1 1 0 0	a2 + a3
1 1 0 1	a0 + a2 + a3
1 1 1 0	a1 + a2 + a3
1 1 1 1	a0 + a1 + a2 + a3

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3.2 Distributed Arithmetic Offset Binary Coding Algorithm

Bo Hong, et al proposed a new algorithm which can reduced the capacity of LUT by half through the use of offset binary coding. Distributed Arithmetic-Offset Binary Code (DAOBC) technique. In this architecture, combination of both Look-up Tables (LUTs) and multiplexers (MUXs) are used for computational purposes. The principle of DA-OBC algorithm is as follows below

$$y(n) = \sum_{k=0}^{N-1} h_k x_k(n)$$

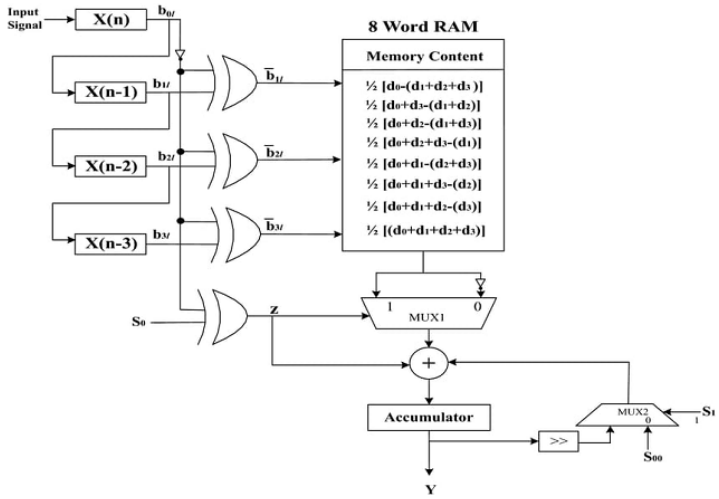
where y(n) is the output data, k(n) is the input data it can be expressed as

$$x_k = \frac{1}{2}\left[x_k - (-x_k)\right]$$

$$= \frac{1}{2}\left[-(x_{k,m-1} - \overline{x_{k,m-1}})\right]$$

$$= \frac{1}{2}\left[-(x_{k,m-1} - \overline{x_{k,m-1}})\right] + \sum_{j=1}^{m-1}\left[\left(x_{k,m-1-j} - \overline{x_{k,m-1-j}}\right)2^{-j} - 2^{-(m-1)}\right]$$

Block Diagram:



LUT Contents:

Address $x_{0j}=0$ $x_{1j}x_{2j}x_{3j}$	LUT Contents	Address $x_{0j}=1$ $x_{1j}x_{2j}x_{3j}$	LUT Contents
000	$\frac{h_0+h_1+h_2+h}{2}$	111	$\frac{h_0+h_1+h_2+h}{2}$
001	$\frac{h_0+h_1+h_2-h}{2}$	110	$\frac{h_0+h_1+h_2-h}{2}$
010	$\frac{h_0+h_1-h_2+h}{2}$	101	$\frac{h_0+h_1-h_2+h}{2}$
011	$\frac{h_0+h_1-h_2-h}{2}$	100	$\frac{h_0+h_1-h_2-h}{2}$
100	$\frac{h_0-h_1+h_2+h}{2}$	011	$\frac{h_0-h_1+h_2+h}{2}$
101	$\frac{h_0-h_1+h_2-h}{2}$	010	$\frac{h_0-h_1+h_2-h}{2}$
110	$\frac{h_0-h_1-h_2+h}{2}$	001	$\frac{h_0-h_1-h_2+h}{2}$
111	$\frac{h_0-h_1-h_2-h}{2}$	000	$\frac{h_0-h_1-h_2-h}{2}$

Table 2: LUT Contents of DA-OBC for 4-tap FIR filter

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IV. Hardware And Software Requirement

4.1 Xilinx Software

Xilinx ISE (Integrated Synthesis Environment) is a discontinued software tool from Xilinx for synthesis and analysis of HDL designs, which primarily targets development of embedded firmware for Xilinx FPGA and CPLD integrated circuit (IC) product families.

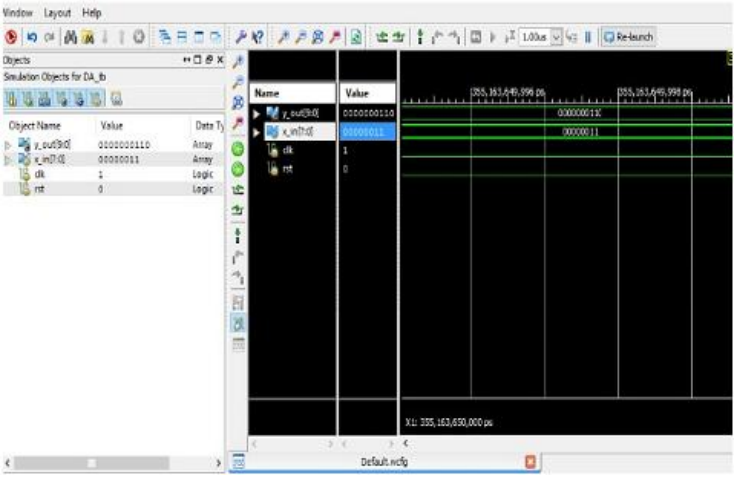
4.2 Verilog HDL

Verilog is a Hardware Description Language (HDL).It is a language used for describing a digital system like a network switch or a microprocessor or a memory or a flip−flop. It means, by using a HDL we can describe any digital hardware at any level. Designs, which are described in HDL are independent of technology, very easy for designing and debugging, and are normally more useful than schematics, particularly for large circuits. Verilog supports a design at many levels of abstraction.

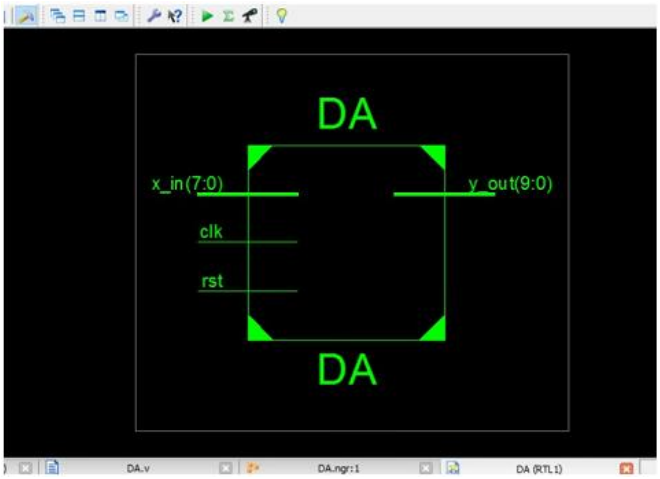
V. Simulation Results

5.1 Distributed Arithmetic

A. Simulation Output



B. RTL Schematic



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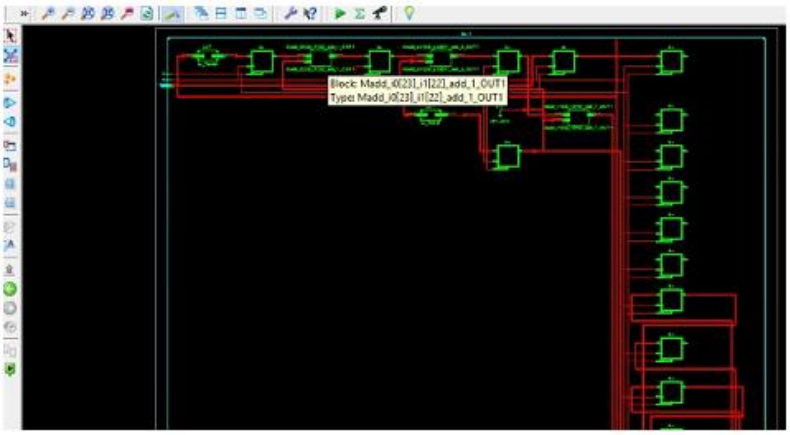
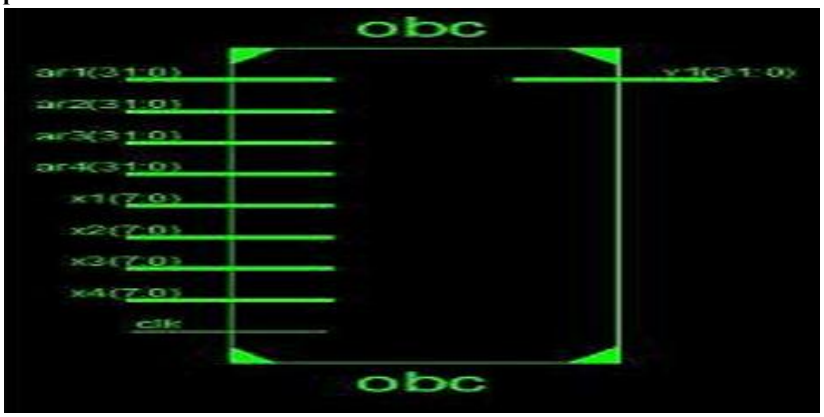
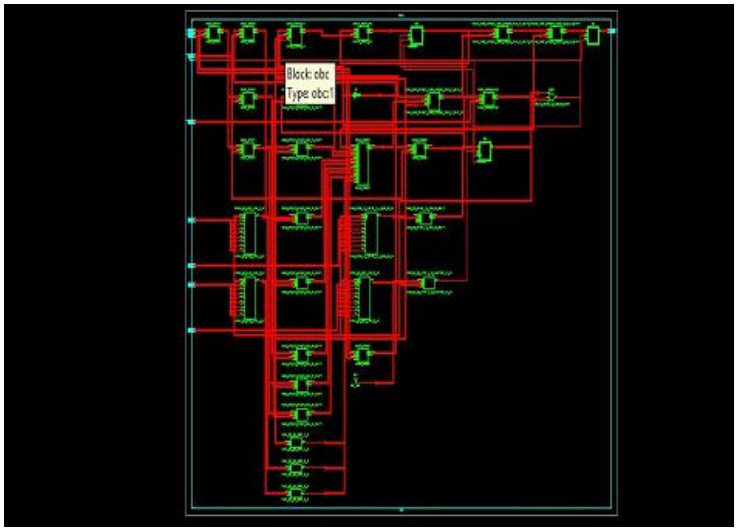


5.2 Distributed Arithmetic Off-Set Binary Coding Algorithms

A. Simulation Output



B. RTL Schematic



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PERFORMANCE PARAMETER	DISTRIBUTED ARITHMETIC	DISTRIBUTED ARITHMETIC OFFSET BINARY CODING
POWER(WATT)	0.082	0.027
GATE DELAY(NS)	0.620	0.600
MEMORY USAGE(KB)	475844	471236
TOTAL CPU TIME	25	12
CLOCK RISE TIME	2.028	1.46

Table: Comparison of DA and DA-OBC Algorithms

VI. CONCLUSION

The Complicated Multiplication – Accumulation operation is converted to the shifting and addition operation when the DA algorithm and DA-OBC algorithms are directly applied to realize FIR filter. However, the size of LUT increases exponentially with each added input address line. This project discusses the design method, selection of structure and the algorithm to reduce the arithmetic complexity of FIR filtering. The main goal is to encompass all the fields that are used in the efficient software realization of filters. This project is an effort to suggest an approach for implementing FIR filter using various algorithm with the help of Xilinx software.

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