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Design of Hybrid Memory Logic Based Built in self-test for Memory Testing

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Abstract: *Microprocessors, microcontrollers, multi-core systems, and multi-processor systems are just a few of the many places where built-in self-test (BIST) modules would be invaluable. Traditional BIST modules cannot remedy the issues in different memories caused by stopped at faults. Errors in memory elements can be detected and fixed with the help of a Hybrid Memory Logic (HML)-BIST, the emphasis of this work. Initial implementations made use of linear feedback shift register (LFSR) modules to generate random test patterns for data writing, address writing, and address reading. Here, non-repetitive random numbers are generated using LFSR using the activity factor. The information in RAM is then compared to the raw data in the original source. The BIST component then fixes the stored data after running the tests. The simulation results showed that the suggested HML-BIST method outperformed the existing methods in terms of area, latency, and power.*

Keywords: BS-LFSR (bits wapped LFSR), LFSR (linear feedback shift register), single stuck-at faults, 8x8 BCD multiplier, Double Dabble algorithm

I. INTRODUCTION

BIST is one of the various methods used to evaluate integrated circuits. It is a device or method that enables a circuitor machine to self-test by combining test rotation with normal system rotation to ensure proper system operation. Figure 1 shows that the BIST design includes the TPG, ORA, and CUT(Circuit Under Test).

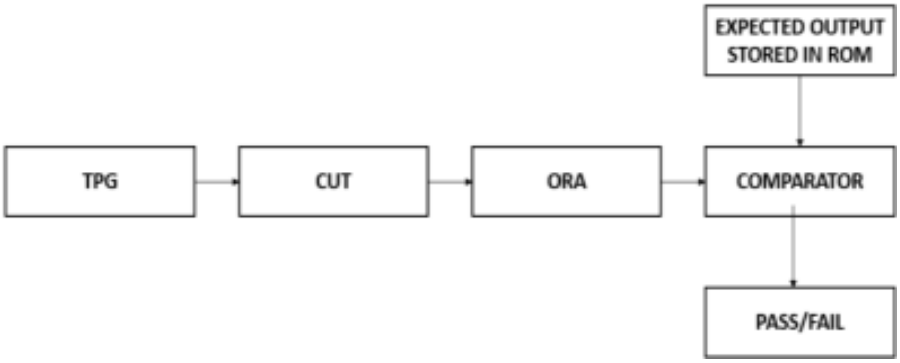

Fig 1: General BIST framework

An energy-efficient TPG and a modified ORA are used in circuit testing in this work. To test, single stuck-at-fault system is utilized. The given article has the following structure. The review of the literature is covered in Chapter II. In chapter III, the System description is covered, which includes conventional LFSR and bit-swapping LFSR as TPG and conventional MISR and modified MISR as ORA.

Because of the fast advancements in integration technologies and large-scale system design - or, to put it another way, because of the birth of VLSI - the electronic industry has seen amazing development over the last two decades. This growth can largely be attributed to the emergence of VLSI. Integrated circuits are finding more and more uses across a variety of industries, including high-performance computing, telecommunications, and consumer electronics, and this trend is continuing at an extremely rapid rate. The needed amount of processing power (or, to put it another way, the

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intelligence) of these applications is often the driving force behind the rapid growth of this sector. [Case in point:] [Case in point:] [Case in point:] [This article provides an overview of the major developments in information technology that are expected to take place during the next several decades. End customers already have access to a certain degree of processing power and mobility thanks to the cutting-edge technologies that are already available. Some examples of these technologies are low bit-rate video and cellular communications. It is anticipated that this tendency will continue, which will have extremely significant ramifications for the design of VLSI and systems. The ever-increasing need for extremely high processing power and bandwidth is one of the most distinctive features of information services (in order to handle real-time video, for example). The fact that information services have a tendency to become more and more personalized (as opposed to collective services such as broadcasting) is the other important characteristic of this trend. This means that the devices must be more intelligent to answer individual demands, and at the same time, they must be portable to allow for more flexibility and mobility[2].

II. LITERATURE REVIEW

[3] illustrates the conception and execution of BIST utilizing the traditional SISR and LFSR. BS approach for low-power BIST is presented in [6], which may decline power utilization by up to 25% when comparing the traditional approach utilized in [3]. By applying BS-LFSR with scan-chain reordering, peak power, as well as average power may both be reduced by up to 65 and 55 percent, correspondingly [7]. In [2], a method for lowering latency and power utilization is called pre-charged XOR with a multiplexer approach. Using clock gating to reduce the test power in BIST system, a novel approach for LFSR-based TPG is put out in [4]. The report [5] examines all significant ATPG approaches to determine which, when combined with BIST, would be best for a particular bit size CUT. The LP-PCBTVG (low power-positioned complements bits test vector generation) method proposed in reference [8,9] declines switching activity and power utilization by rising association in test vectors. In [10], a novel weighted pseudo-random TPG and reseeding approach for low power (LP) scan-based BIST is introduced. The pass transistor-based LFSR design has the lowest power consumption and the fewest transistors, according to the examination of several LFSR designs for implementing BIST in [11]. For all BIST applications, [12] provides an inexpensive, low-power ring oscillator-based TPG. NLFSR, which uses less power on- chip than LFSR by more than 80%, is utilized as TPG in [13]. A novel method for achieving higher fault coverage is presented in [14]. In [15], the toggling rate estimation approach is tested using LUT circuits and benchmark gate levels. MISR has four structural representations in [16], and it was shown that modular MISR is more effective than other reconfigurable MISRs in terms of execution speed and gate utilization.

III. SYSTEM DESCRIPTION

Since the beginning of this decade, Very Large-Scale Integration (VLSI) has seen a significant increase in the integration density it can achieve. Because of this, the system-on-chip was realized [17]. When testing VLSI chips with external hardware, the process may be exceedingly challenging. It is highly challenging to test such VLSI circuits because of the large amount of test data that is needed. The traditional testing technique involves storing a significant quantity of test data outside in order to test the Circuit Under Test (CUT) [18]. The BIST is an alternate testing instrument that may be used outside. The development of test patterns and the analysis of responses are both carried out inside the chip itself in BIST. In addition to these advantages, using BIST may also raise the testing speed while simultaneously improving the testing quality [19]. VLSI, or very large scale integration, is a kind of cell technology that is based on semiconductors and is used to construct integrated circuits by merging thousands of transistors. Both the microprocessor and the microcontroller are examples of devices that are based on VLSI.

Integrated circuits may include a central processing unit, random access memory, read only memory (ROM), and other logic devices [20]. The VLSI technology integrates several kinds of devices into a single chip. The advancement of VLSI technology enables embedded systems to be created for specialized applications at prices that are within reach of all members of the society. The primary necessity of the VLSI design is to assess the dependability of the produced goods [21]. The approach of structured design is used for the purpose of making testing of VLSI circuits easier. A semiconductor design that cannot be tested may need more time to test and develop. One of the most important steps in the design and production of integrated circuits is sorting the chips on the wafer based on their quality. The quality of

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the goods and the degree of satisfaction experienced by customers are directly linked to early detection of defective integrated circuits (ICs) during manufacturing.

The methodologies Design for Testing (DFT) [22] and BIST are used to test the chip during the design stages to determine whether or not it is stuck-at-fault one hundred percent of the time. DFT is equipped with a number of different methodologies, including as the scan design method, on-chip hardware for the development of test patterns, and data compression methods, that may boost controllability and observability. The BIST scheme is formed by combining a number of different DFT approaches [7]. Combined test pattern creation, built-in evaluation, self-test, partitioning, multiplexer test point insertion, serial scan, and random test pattern are some of the key BIST techniques. At the design stage itself, there are a variety of methods available to identify any defects that may exist in the chip [8]. During the design stage of the chip itself, design verification processes and computer assisted design procedures are used in order to locate the error that has been introduced. The production test will be able to determine whether or not there is an error in the manufacturing process. It is not uncommon for the chip to develop physical faults, which, if left unchecked, will cause the chip to fail to perform the function for which it was designed [9].

The most prevalent types of defects that might develop include bulk silicon flaws, substrate mounting defects, substrate surface faults, bonding defects, particle contamination, temperature mismatch electrical stability, oxide defects, and metallization defects [10]. The stuck at fault model offers an explanation of the underlying physical reasons of the stuck at '0' and trapped at '1' faults. These faults are denoted by the notation "0" and "1," respectively. The stuck at fault model is sufficient on its own to discover the many different kinds of flaws that were discussed in the previous paragraph. The stuck at fault idea is used to generate test patterns [11], which are then executed. BIST is an abbreviation that stands for "back-instruction self-test," and it refers to a technique for testing a circuit while the circuit itself is being tested. This technique involves including the testing operations directly into the CUT. The following is a list of the significant contributions that this work makes:

• The implementation of an HML-BIST by making use of LFSR modules and incorporating activity controlling.

• The design of LFSR-based random number generators for write address, read address, and write data, in which activity factor is utilized to generate non-repeated random numbers. These random number generators will be used for write address, read address, and write data.

• The implementation of a space comparator in order to determine the errors that are present in the data that is stored in memory.

The process of inspecting the circuit being tested is the foundation of the HML-BIST algorithm that has been proposed. Memory, the test pattern generator, and the RAM output response analyzer are three of the most significant structures that make up the BIST architecture. The standard implementation of BIST can be broken down into nine distinct parts.

Table 1. BIST Algorithm

Identify the number of inputs (N) and outputs of the circuit that is being tested as the first step.
Generate 2N different test patterns as the second step.
The next step is to store each test pattern's real output in the ROM memory.
Step four involves applying the test pattern 1 and analyzing the results using the output response analyzer.
In the fifth step, the comparator examines the output signature to determine whether or not it matches the golden signature.
Step 6: If there isn't a problem, proceed to step 4 to check for the next test pattern.
Step 7: Determine whether or not the test pattern has reached its conclusion.
Step 8: If the circuit that is being tested does not show any faults during the whole test pattern, declare that the circuit is OK.
Step 9: Determine whether the CUT was a success or a failure.

The HML-BISTapproach that has been suggested using LFSR-based activity factor regulating may be shown in Figure 1. The test pattern generator, which makes use of LFSR, the space comparator-based output analyser, and the random access memory are the three essential components of the BIST (RAM). The generation of the necessary test pattern for the circuit that is now being evaluated is the job of the test pattern generator. In the realm of test pattern 3 generators, some examples are the LFSR, the counter, and RAM that already has testing data stored in it. The Response Analyzer is

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a sort of Comparator that retains model outputs for the purpose of comparing them with the actual outputs of the circuit that is being tested. A circuit known as the test controller is responsible for sending command signals to the test pattern generator in order to make test patterns available for testing. In addition to this, it sends signals to the space comparator, which causes it to compare the current output to the output that has previously been stored

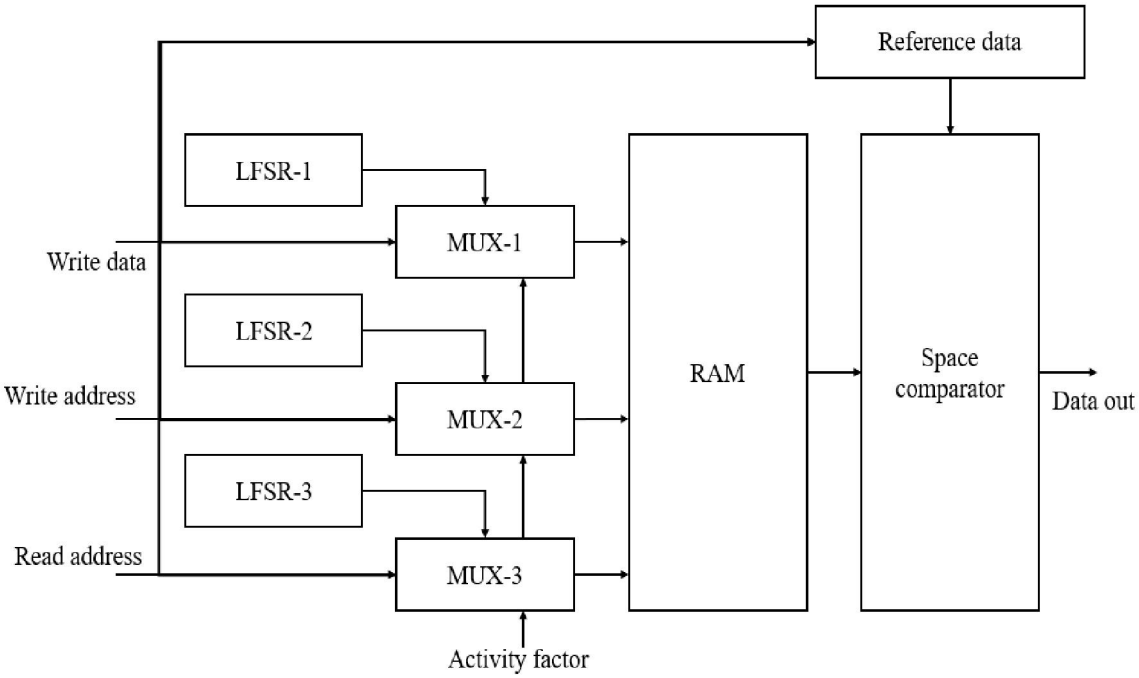

Figure 2. Proposed HML-BIST architecture.

The RAM is where all of the functions relating to the test are carried out. The fault model is developed via the process of coding. By writing code in Xilinx software, it is possible to generate a stuck at 1 fault as well as a stuck at zero error. The output of the output space comparator provides information that may be used to diagnose the problem. For a fault that is stuck at 1, all of the output may be high, whereas for a fault that is trapped at 0, all of the output could be low. Therefore, the output space comparator may be used in order to investigate the nature of the issue. The BIST incorporates both the circuit that generates the test pattern and the circuit that is being tested. When producing the test vector for the circuit that is being tested, LFSR is an essential component to have. In the LFSR-based test pattern generation that is being suggested, a total of 12 outputs are produced. The 12 outputs of the LFSR are converted by the isolation circuit into four inputs that are then used by the s27 sequential logical circuit.

The circuit being tested accepts as inputs the four outputs that are produced by the isolation circuit, processes those inputs, and then produces just one output. The output response analyzer is responsible for doing analysis on the CUT's outputs. In order to determine whether or not the circuit is functioning properly, the output response analyzer compares the output of the CUT with memory. The circuit that is being tested will, during its usual mode of operation, receive signals from the input sources and create output signals that are sent to other devices. It will not accept any signals that are connected to BIST. Only the CUT will be the component that gets signals from the test pattern generator while the BIST is operating. The response analyzer will be used to examine how the CUT responds to various stimuli. The signals received from the response analyzer are compared with the reference signals that have previously been saved in the chip. The comparator is responsible for producing error signals. The error signals reveal whether or not the circuit being tested is functioning properly.

The approach known as BIST is included into the embedded system. When creating the embedded system for the BIST approach, there are four characteristics that need to be taken into consideration. These include hardware overhead, test set size, fault coverage, and performance overhead. If there are any mistakes at all in the test pattern that is generated by the test pattern generator, the space comparator will not provide an error signal and will instead show that the CUT is

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error free. Aliasing or masking are two names that are sometimes used to refer to this unwanted phenomenon. The term "test set size" refers to the total number of test patterns that are generated by the test pattern generator. If the size of the test set is increased, then the fault coverage will increase as well. If the size of the test set is too low, then it will not be able to cover all of the errors. The term "hardware overhead" refers to the supplementary hardware that must be installed in order to implement BIST. When implementing BIST in an embedded system, having additional hardware is not something that is ideal. In the BIST technique, it is preferable to use a smaller number of pieces of hardware for a larger circuit that is being tested. The use of BIST approach has the potential to sometimes interfere with the typical operation of the circuit that is being tested. During the usual functioning of the CUT, there is the possibility of a delay in responding. The term "performance overhead" refers to this unwanted quality. Because of this, there is a possibility that the consequences will be more severe than the hardware overhead. For a more successful application of the BIST technique in embedded systems, the aforementioned four characteristics need to be taken into consideration.

When it comes to testing VLSI circuits, there are a plethora of test pattern options at your disposal. The researchers are generating a large number of new control methods each day and contributing a significant amount of labor to the study. Pseudo-random pattern is formed by a string of ones and zeros that are entered in a haphazard manner. This pattern is utilized as a testing vector for digital circuits. Pseudo-random pattern generator is the primary use for the Low Frequency Shaping Register (LFSR). This method creates a greater variety of patterns than the ATPG bus while still producing fewer patterns than pseudo pattern generation. When compared to other methods, the production of pseudo-random patterns often requires a longer amount of time. Additionally, in comparison to previous strategies, this method calls for a smaller amount of hardware, a lower performance overhead, and a reduced amount of design work.

In order to produce the pseudo-random pattern, the LFSR is put to use. The length of the string, also known as the seed, is either comparable to or less than the length of the LFSR. In terms of LFSR, the seed and test vectors may be obtained by solving a linear set of algebraic equations. Figure 2 depicts a general example of the LFSR's architectural make-up.

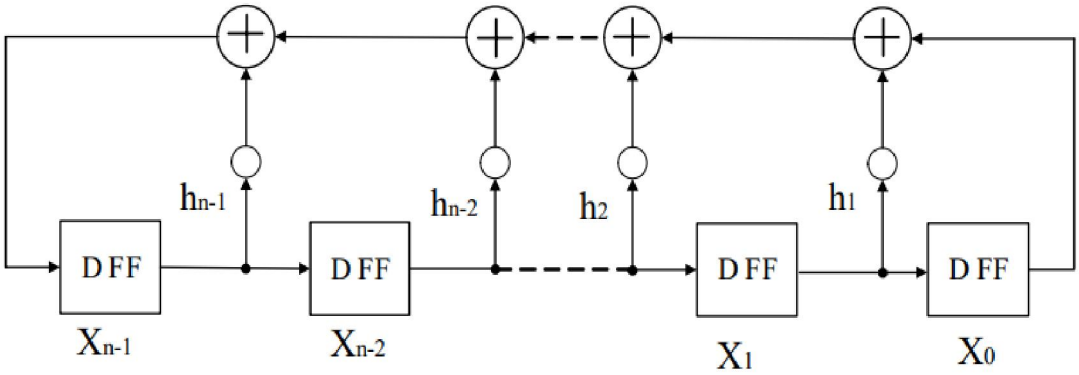

Figure 3. A standard LFSR structure.

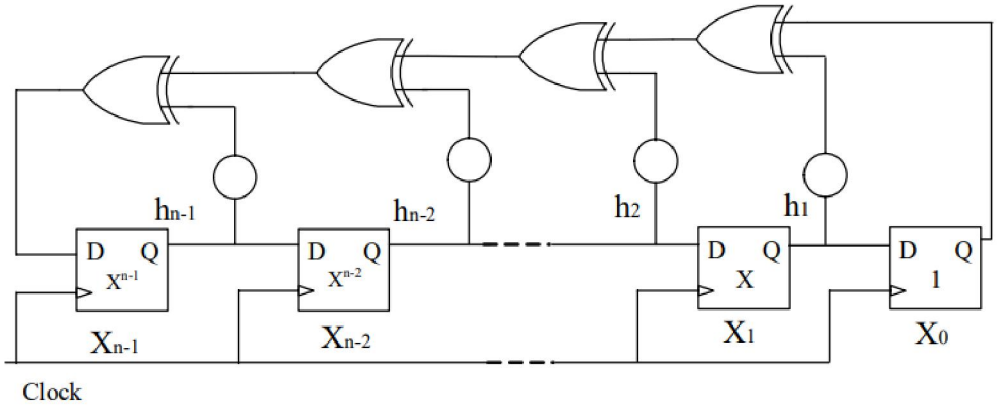

Figure 4.n-stage LFSR with actual digital circuit

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The test pattern is generated by a significant number of D flip flops, which make up the majority of the LFSR. In order to provide feedback and achieve pseudo random pattern creation, the outputs of D flip flops are mixed with the outputs of other D flip flops in a certain sequence. The LFSR may be realized by the use of the actual digital circuit. Figure 3 depicts the n stage LFSR in its entirety.

The construction of an n-stage LFSR that is capable of producing n output lines using the outputs of a D flip-flop. In addition, the output of one D flip flop is mixed with the output of another D flip flop using an XOR gate, and the result is fed back into the first D flip flop. The clock pulse for all of the D flip flops originates from the same location. It is possible to produce the necessary Pseudo pattern from the LFSR using the appropriate connections for the EXOR gate.

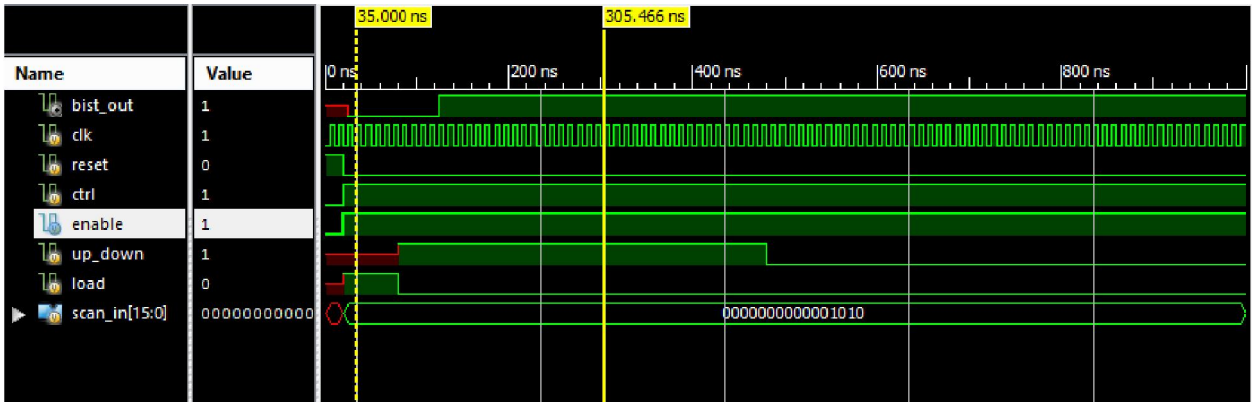

Figure 6: Simulation

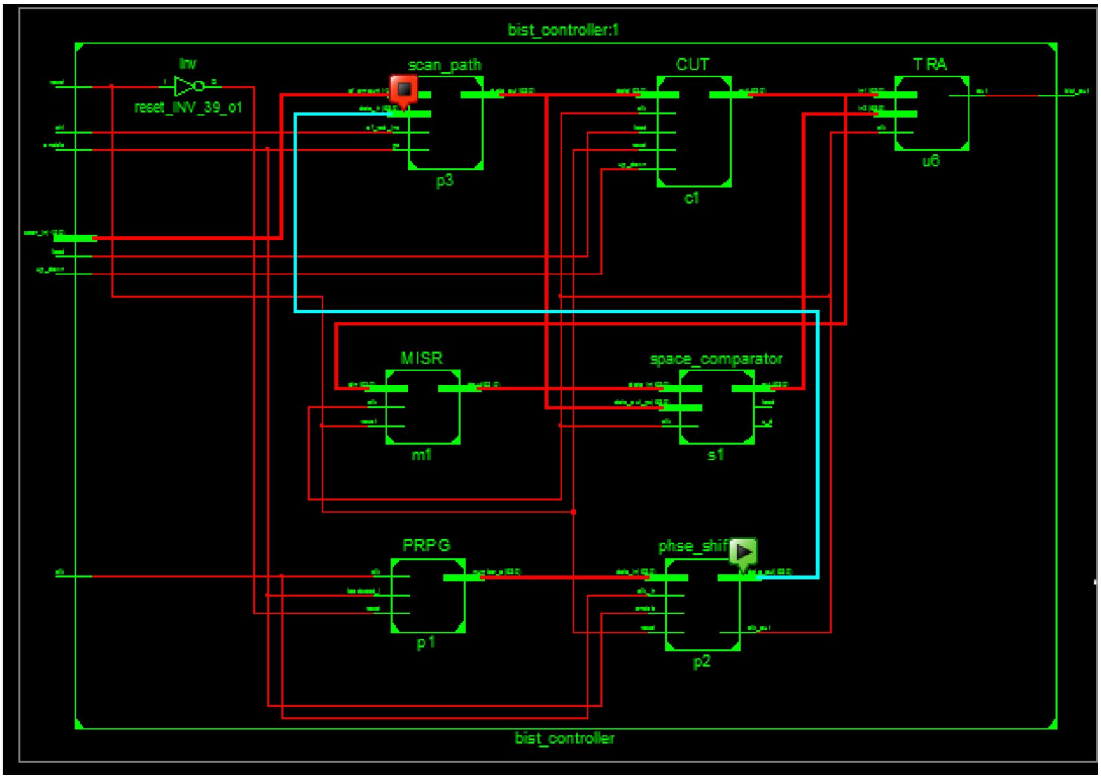

Figure 7: RTL schematic

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Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	768	35200	2%
Number of Slice LUTs	6285	17600	35%
Number of fully used LUT-FF pairs	612	6441	9%
Number of bonded IOBs	23	100	23%
Number of BUFG/BUFGCTRLs	2	32	6%

Figure 8: Design summary

```
Data Path: u6/out to bist_out
                                   Gate     Net
  Cell:in->out      fanout         Delay    Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   FD:C->Q               2         0.232    0.283  u6/out (u6/out)
   OBUF:I->O                       0.000           bist_out_OBUF (bist_out)
  ----------------------------------------
  Total                            0.515ns (0.232ns logic, 0.283ns route)
                                           (45.0% logic, 55.0% route)

--------------------------------------------------------------------------------
```

Figure 9: Time summary

Device		On-Chip	Power (W)	Used	Available	Utilization (%)
Family	Virtex6	Clocks	0.000	1	--	--
Part	xc6vlx75tl	Logic	0.000	46	46560	0
Package	ff484	Signals	0.000	122	--	--
Temp Grade	Commercial	IOs	0.000	52	240	22
Process	Typical	Leakage	1.065			
Speed Grade	-1L	Total	1.065			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	0.900	0.435	0.000	0.435
Vccaux	2.500	0.045	0.000	0.045
Vcco25	2.500	0.001	0.000	0.001
MGTAVcc	1.000	0.303	0.000	0.303
MGTAVtt	1.200	0.213	0.000	0.213

Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	8 to 11
Custom TJB (C/W)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	2.7	82.1	52.9

Supply Power (W)	Total	Dynamic	Quiescent
	1.065	0.000	1.065

Figure 10: Power summary

3.1 Proposed Results

The Xilinx ISE software was utilized during the creation of each and every BIST design. This piece of software is capable of producing two distinct types of outputs, namely simulation and synthesis. The findings of the simulation allow for a comprehensive investigation of the BIST architecture with regard to the various combinations of input and output byte levels. A simple decoding technique can be approximated by applying a large number of different combinations of inputs and watching a wide variety of outputs while doing a simulation study of correct encoding. As a direct consequence of the findings of the synthesis, the utilization of space in proportion to the number of transistors will be carried out. In addition, a time summary will be produced in reference to the numerous path delays, and a power summary will be prepared making use of the static and dynamic power consumption. Both of these summaries will be obtained.

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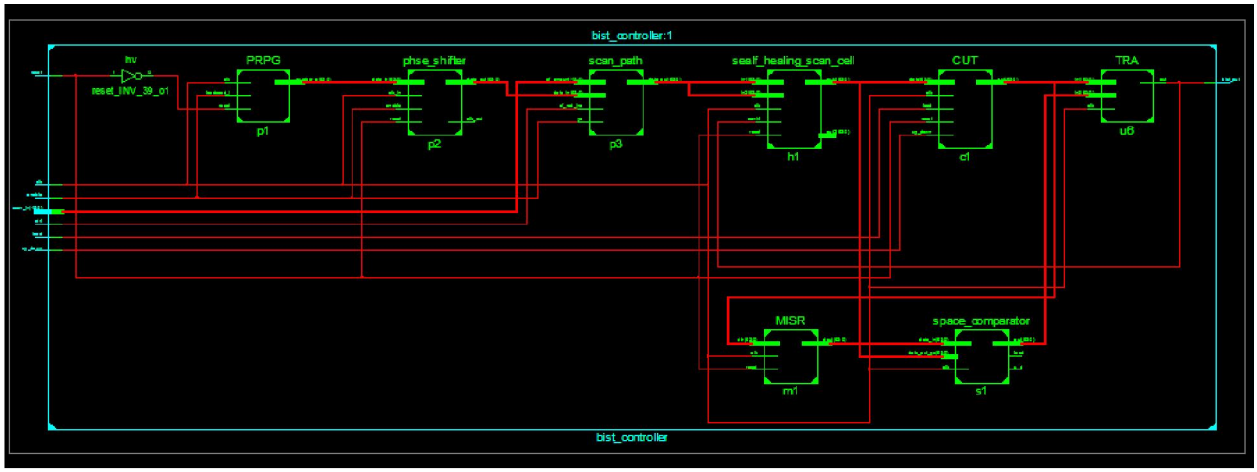

Figure 10: Proposed schematic

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	512	35200	1%
Number of Slice LUTs	12142	17600	68%
Number of fully used LUT-FF pairs	348	12306	2%
Number of bonded IOBs	24	100	24%
Number of BUFG/BUFGCTRLs	2	32	6%
Number of DSP48E1s	1	80	1%

Figure 11: Design summary.

The design (area) summary of the suggested method can be found in Figure 4. In this case, the proposed technique makes use of a relatively small portion of the available slice LUTs, specifically 12142 of the total 17600. In addition, the proposed approach uses 512 of the 35200 slice registers rather than the full capacity of all of them. In addition, the proposed approach uses 348 of the completely utilised LUT-FF out of a total of 12306 that are available. In addition, out of the total of 32 buffers that are accessible, the proposed solution only uses two of them.

```
Data Path: u6/out to bist_out
                                   Gate     Net
  Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   FD:C->Q               1   0.232   0.279  u6/out (u6/out)
   OBUF:I->O                 0.000          bist_out_OBUF (bist_out)
  ----------------------------------------
  Total                      0.511ns (0.232ns logic, 0.279ns route)
                                     (45.4% logic, 54.6% route)

--------------------------------------------------------------------------------
```

Figure 12: Time summary

The timing breakdown of the proposed technique is presented in Figure 5. In this instance, the suggested procedure required a total of 0.511ns of time delay, of which 0.232ns of delay was logical and 0.279ns of delay was route.

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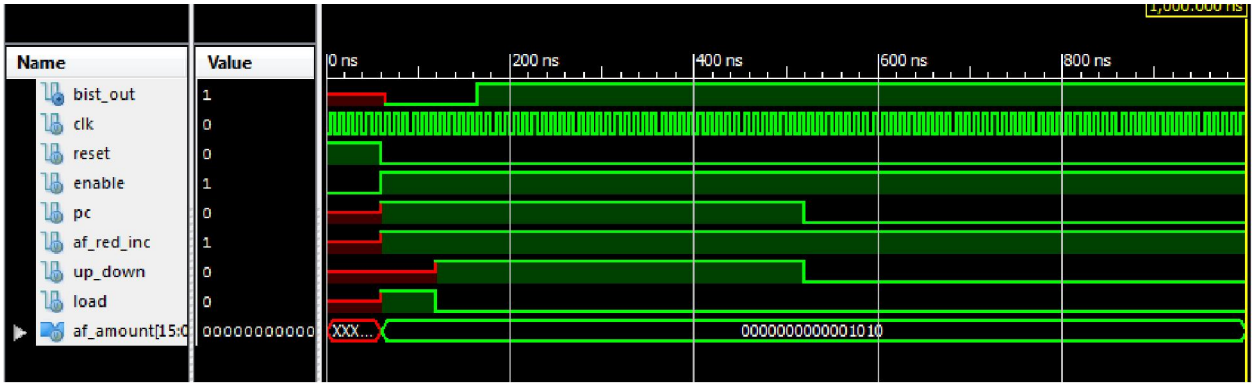

Figure 13: Simulation outcome.

Figure 6 illustrates the results of running the simulation using the proposed approach. In this context, the input data pins are denoted by the following symbols: clock (clk), reset, enable, program_counter (pc), activity_factor_reduction_increment (af_red_inc), up_down, load, and af_amount. Additionally, the output pin is denoted by the symbol bist_out. The system is initialized to zero during the active high reset, and it begins its normal operation during the active low reset. When the active low enable, PC signal is present, the system is disabled, and when the active high enable, PC signal is present, the system begins operating normally. In the BIST environment, the af_amount will be loaded if the load is determined to be active high. In addition, an increase in the active value of af_red_inc led to an increase in the activity factor, while a decrease in the active value of af_red_inc led to a decrease in the activity factor. In addition, when the up_down input was active with a high value, the counting was incremented, and when it was active with a low value, the numbering was decremented. In conclusion, a BIST fail condition is indicated when the active low value of bist_out is low, while a BIST pass condition is indicated when the active high value of bist_out is high.

Device	
Family	Virtex6
Part	xc6vlx75tl
Package	ff484
Temp Grade	Commercial
Process	Typical
Speed Grade	-1L

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	--	--
Logic	0.000	46	46560	0
Signals	0.000	122	--	--
IOs	0.000	52	240	22
Leakage	1.065			
Total	1.065			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	0.900	0.435	0.000	0.435
Vccaux	2.500	0.045	0.000	0.045
Vcco25	2.500	0.001	0.000	0.001
MGTAVcc	1.000	0.303	0.000	0.303
MGTAVtt	1.200	0.213	0.000	0.213

Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	8 to 11
Custom TJB (C/W)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	2.7	82.1	52.9

Supply Power (W)	Total	Dynamic	Quiescent
	1.065	0.000	1.065

Figure 14: Power summary.

Figure 14 presents the power consumption report that was generated by the propsed HML-BIST. In this scenario, the proposed HML-BIST had a power consumption of 1.065 watts. The comparative analysis of the performance of the various BIST controllers is presented in Table 1. In this case, the proposed HML-BIST resulted in superior (reduced) performance in terms of the number of LUTs, slice registers, LUT-FFs, time-delay, and power consumption when compared to existing approaches such as MBIST [22], PSRG-BIST [23], and FT-BIST [24]. This was the case because the proposed HML-BIST used fewer slice registers. Figure 15 also provides a graphical overview of the performance comparisons that were conducted.

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Table 2. Performance evaluation.

Metric	MBIST [22]	PSRG-BIST [23]	FT-BIST [24]	Proposed HML-BIST
Slice Registers	784	734	673	512
LUTs	18367	17352	15327	12142
LUT-FFs	826	736	635	348
Time delay (ns)	0.927	0.836	0.726	0.511
Power consumption (w)	32.482	24.1939	16.937	1.1065

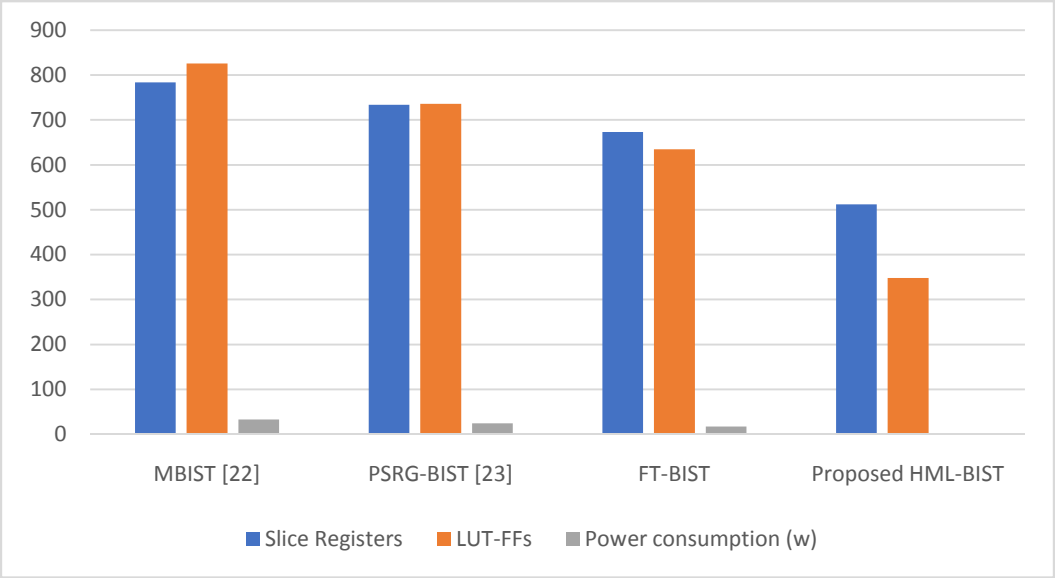

Figure 15. Graphical representation of performance evaluation.

IV. CONCLUSION

The primary objective of this effort is to create a working version of an HML-BIST, a tool that can detect and address flaws in the components of memory systems. LFSR modules were initially implemented so that a random test pattern could be generated for each of the three operations of write address, read address, and write data. In this particular instance, the LFSR algorithm is applied in order to generate non-repeated random numbers by utilizing the activity factor. After that, the information in memory is put through a space comparator so that it may be compared with the information coming from the initial source. After that, the BIST module will correct the memory for a number of different test scenarios. The simulations demonstrated that the proposed BIST method was superior to other approaches in terms of the amount of space it required, the amount of time it took, and the amount of power it consumed

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