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Design of Low power Low Offset Dynamic latch Comparator using DTMOS Technique

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Abstract: *Analog to Digital converters plays an essential role in signal processing and medical applications. SAR ADC is best suited for biomedical applications because of its low power and medium resolution. Low power dynamic comparators are essentially desired in the design of SAR ADC. In this paper, a lowpower dynamic type latch comparator is designed which is based on Dynamic Threshold Metal Oxide Semiconductor (DTMOS) technique to reduce the power dissipation which is achieved by reducing the supply voltage. The circuit has been implemented atthe supply voltage of 0.8 V. The simulations for this comparator are carried out in CADENCE SPECTRE using 45nm CMOS technology. The simulation outcomes validate that the designed dynamic latch comparator with DTMOS techniques is 20% morepower saving in comparison to the conventional comparator. Thetotal power consumption is as low as 156.18nW which makes it suitable for low-power bio-medical applications.*

Keywords: Dynamic latch comparator, Low power, SAR- ADC, DTMOS..

REFERENCES

[1]. Allen, P.E., and Holberg, D.R., "CMOS analog circuit design", Oxford: Oxford University Press, 2002.
[2]. B. Goll and H.Zimmerman, " A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," IEEE Trans Circuits Syst.II, Exp Briefs, Vol. 56, no.11, pp. 810-814, Nov. 2009.
[3]. Witch, B. Nirschl, T. and Schmitt-Landsiedel, D., "Yield and speed optimization of a latch-type voltage sense amplifier", IEEE Jounal of Solid State Circuits, Vol. 39, no.7, pp. 1148-1158, 2004.
[4]. Ragab, K., Chen, L., Sanyal, A., and Sun , N., "Digital background calibration for pipelined ADCs based on comparator decision time quantization ", IEEE Trans Circuits Syst.II, Exp Briefs, Vol. 62, no.5, pp. 456-460, 2015.
[5]. Goll, B., and Zimmermann, H., "A 65nm CMOS comparator with modified latch to achieve 7GHz/1.3W at
[6]. 1.2 V and 700MHz/47 lW at 0.6 V", IEEE International Solid-State Circuits Conference (ISSCC) Digest Technical Papers, pp. 328–329, 2009.
[7]. Kim, Jaeha, Kevin D. Jones, and Mark A. Horowitz, "Fast, non-monte carlo estimation of transient performance variation due to device mismatch", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 7, pp. 1746-1755, 2010.
[8]. Katyal, V., Geiger, R. L., and Chen, D. J., "A new high precision low offset dynamic comparator for high resolution high speed ADCs", In IEEE Asia Pacific Conference on Circuits and Systems, pp. 5-8, 2006.
[9]. Maymandi-Nejad, M., and Sachdev, M., "1-bit quantizer with rail to rail input range for sub-1 V Σ-Δ modulators", Electronics Letters, vol. 39, pp. 894–895, 2003.
[10]. Lu, J. and Holleman, J., "A low-power high-precision comparator withtime-domain bulk-tuned offset cancellation", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, pp. 1158-1167, 2013.
[11]. Dubey, Avaneesh K., and R. K. Nagaria, "Enhanced Gain Low-Power CMOS Amplifiers: A Novel Design Approach Using Bulk-Driven Load and Introduction to GACOBA Technique," Journal of Circuits, Systems and Computers (JCSC), vol. 27, no. 13, 2018.
[12]. Hassanpourghadi, M., Zamani, M., and Sharifkhani, M., "A low-power low-offset dynamic comparator for analog to digital converters", Microelectronics Journal, vol. 45, pp. 256-262, 2014.

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[13]. Chiang, S. H. W., "Comparator offset calibration using unbalanced clocks for high speed and high power efficiency", Electronics Letters, vol. 52, pp. 1206-1207, 2016.

[14]. Dubey, Avaneesh K., and R. K. Nagaria, "Optimization for offset and kickback-noise in novel CMOS double-tail dynamic comparator: A lowpower, high-speed design approach using bulk-driven load," Microelectronics Journal, vol. 78, , pp. 1-10, 2018.

[15]. Kandala, M., and Wang, H., "A 0.5 V high-speed comparator with railto-rail input range", Analog Integrated Circuits and Signal Processing, vol. 73, pp. 415-421, 2012.

[16]. Mesgarani, A., Alam, M. N., Nelson, F. Z., and Ay, S. U., "Supply boosting technique for designing very low-voltage mixed signal circuits in standard CMOS", In 53rd IEEE international midwest symposium on circuits and systems, pp. 893–896, 2010.

[17]. T.B Cho and P.R. Gray, "A 10b, 20 Msamples/s, 35mW pipeline A/D converter," IEEEJ.Solid -State Circuits, Vol.30, no.3, pp.166-172, Mar.1995.

[18]. Khateb, F., Dabbous, S.B.A., Vlassis, S.: A survey of non- conventional techniques or low-voltage low-power analog circuit design. Radioengineering 22, 415–427, 2013.

[19]. Yan, S., Sanchez-Sinencio, E.: Low voltage analog circuit design techniques: a tutorial.IEICE Trans. Analog Integr. Circ. Syst. E00-A(2), 2000.

[20]. Khateb, F., Khatib, N., Koton, J.: Novel low-voltage ultra- low power DVCC based on floating-gate folded cascade OTA. Microelectron. J. 42, 1010–1017, 2011.

[21]. Farshidi, E., Keramatzadeh, A.: A new approach for low voltage CMOS based on current-controlled conveyors. IJE Trans. B: Appl. 27, 723–730, 2014.

[22]. Ramirez-Angulo, J., Lopez-Martin, A.J., Carvajal, R.G., Chavero, F.M.: Very low-volatge analog signal processing based on quasi-floating gate transistors. IEEE J. Solid-State Circ.39, 434–442, 2003.

[23]. Fallah, M., MiarNaimi, H.: A novel low voltage, low power and high gain operational amplifier using negativeresistance and self cascode transistors. IJE Trans. C: Aspects 26, 303–308, 2013.

[24]. Assaderaghi, F., Sinitsky, D., Parke, S.A., et al.: Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low- voltage VLSI. IEEE Trans. Electron Devices 44, 414–422, 1997.

[25]. Assaderaghi, F., Parke, S.A., Sinitskyd, D., Bokor, J., Ko, P.K., Hu, C.: Dynamic threshold-voltage MOSFET (DTMOS) for very low-voltage operation. IEEE Device Lett.15, 510–512, 1994.

[26]. Shieh, M.S., Chen, P.S., Tsai, M.J., Lei, T.F.: A novel dynamic threshold voltage MOSFET (DTMOS) using heterostructure channel of Si1 yCy interlayer. IEEE Electron Device Lett.26, 740–742, 2005.

[27]. Kang, S.M., Leblebici, Y.: CMOS Digital Integrated Circuit : Analysis and Design. TMH, 2008.