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Design of Low Power 2-4 Mixed Logic Line Decoders

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Abstract: *This brief introduces a mixed-logic design method for line decoders, combining transmission gate logic; pass transistor dual-value logic, and static complementary metal-oxide semiconductor (CMOS). Two novel topologies are presented for the 2–4 decoders a 14 transistor topology aiming on minimizing transistor count and power dissipation and a 15transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. Furthermore, four new 4–16 decoders are designed by using mixed-logic2–4 pre decoders combined with standard CMOS post decoder. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulation sat 32 nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.*

Keywords: Low Power, 2-4 Mixed Logic, Line Decoders, CMOS, Transistor Topology

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