IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 5, Issue 2, September 2025
Impact Factor: 7.67

Leakage Power Reduction in Low-Process-Technology VLSI Circuits Using Regulated Cross-Coupled and Split Inverter Techniques

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Abstract: *This work presents a novel power-efficient level shifter design that integrates a regulated cross-coupled (RCC) network with a SAPON-based split inverter to achieve significant reductions in both leakage and dynamic short-circuit power. The RCC network effectively minimizes power loss in the pull-up path, while the split inverter at the output ensures reduced short-circuit current during switching transitions. To further enhance performance, a modified split inverter with an added load capacitor is employed, which accelerates switching speed, stabilizes node voltages, and improves overall energy efficiency. The proposed design operates reliably in the sub-threshold region, accommodating voltage levels from 0 V to 0.5 V for 50 nm technology and 0 V to 0.9 V for 90 nm technology, while achieving nearly 31–32% power savings compared to conventional level shifter designs. Comprehensive LTspice simulations validate the functionality, demonstrating low leakage currents, high-speed transitions, and stable operation across multiple input cycles, indicating its suitability for modern low-power VLSI systems and multi-voltage domain applications.*

Keywords: Level shifter, split inverter, regulated cross-coupled network, threshold voltage, leakage reduction, short-circuit power.

DOI: 10.48175/IJARSCT-29038