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Systems used for Power-Constrained Testing of Digital Circuits: A Review of DFT and Power Management Integration

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Abstract: *The low power consumption is a critical demand in the design and testing of the modern VLSI architecture and a System on a Chip (SoC). Under a test mode, untamed switching activities can make the power requirements of the device far higher than that of being functional thereby creating a lot of thermal stress and even damaging the circuit and making tests expensive in the process. Several power-conscious test methods have been developed to counter these issues and they target low switching activity testing and regulation of peak power without sacrificing fault coverage. They encompass state-of-the-art test vector optimization including: vector reordering, compression, and X-plus scan chain reordering and clock gating plans. Energy efficiency is further increased with low-power Built-In Self-Test (BIST) design and with adaptive testing whose accuracy depends on monitoring of real-time power. Scalable and power-efficient tests with large and complex systems are possible through hierarchical and modular design Design-for-Test (DFT) methodologies. Real-time power adaptation can be done through techniques such as Dynamic Voltage and Frequency Scaling (DVFS) and AI-based algorithms and metaheuristic methods can be used to plan tests and optimize testing. This review expounds on such options in detail, with synthesis and power management as a major enabling factor in robust, scalable, and energy-efficient testing in next-generation digital systems.*

Keywords: Power-constrained testing, Lower-Power VLSI circuits, System-on-Chip (SoC) Testing, Design-for-Test (DFT), Built-In Self-Test (BIST), Test power management

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