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Conditional Bridging Low-Power High-Speed Sense-Amplifiers Over Flip-Flops

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Abstract: *Along with space and speed, power consumption is regarded as a significant difficulty in contemporary VLSI design. The flip-flop is an integral part of digital systems. We compare and contrast four distinct flip-flop topologies in sub-threshold operation: IP-DCO, MHLFF, CPSFF, & CPFF. These topologies encompass both pulse-triggered and conditional techniques. Sub threshold technology has recently made it feasible to implement applications with very low power consumption. This technology's benefit is that it reduces the power consuming flip-flops. When operating at the same frequency, a sub threshold circuit uses less power than a strong inversion circuit. The 18nm technology used by Tanner in cmos is used for design. At a power supply voltage of 1V, the flip-flops are examined from every angle, and characteristics including average power, power delay product, and power delay are measured.*

Keywords: Sub Threshold Technology, Flip Flop, Low Power

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