

Adaptive Forward Body Bias Voltage Generator using 45NM Technology

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Abstract: In both analog and digital circuits, the performance heavily relies on the threshold voltage (or turn-on voltage) of transistors. However, technology scaling doesn't proportionally reduce the threshold voltage relative to the aspect ratio of transistors. To tackle this challenge, the forward body bias (FBB) technique is employed to lower the threshold voltage of transistors. Thus enhancing device operating speed and enabling operation at lower supply voltages, albeit at the expense of forward biasing the bulk-drain or bulk-source junction. To overcome this challenge, an adaptive FBB voltage generator was designed to track the process and temperature variations by adjusting its output voltage accordingly. Notably, this adaptive FBB voltage also aids in reducing static leakage current through the bulk in comparison to a fixed FBB voltage. The proposed design has been simulated in 45nm Cadence Virtuoso, use of such newer technology nodes typically offers advantages over older nodes like 90nm in terms of performance, power efficiency, reliability and integration. When implemented in a 45nm technology node, the circuit retains its output without alteration, resulting in a reduced area, thereby providing an advantage in terms of area reduction. It is envisioned that integrating this solution into the digital signal processing (DSP) curriculum could elevate operating speeds and peripheral circuit performance of memory technologies such as SRAM, DRAM and others) thereby accelerating the read path and decreasing access time. Furthermore, analog circuits can leverage this solution to boost the transconductance of transistors by minimizing the threshold voltage

Keywords: forward body bias, threshold voltage, adaptive FBB, fixed FBB, static leakage