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Design and Implementation of Low Power Comparator Based Flash ADC

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Abstract: *This project describes the design of a high-speed latched comparator with a 6- bit resolution, full-scale voltage of 1.6 V, and a sampling frequency of 250 MHz. The comparator is designed in a 0.35 µm CMOS process with a supply voltage of 3.3 V. The comparator is designed for time-interleaved band-pass sigma-delta ADC. Due to the nature of the target application, it should be possible to turn off the components to avoid static power consumption. The comparator of this design implements the turn-off technique when it is not in use. The settling time of the comparator is less than half the clock cycle which means it does not affect the functionality of the band-pass sigma-delta ADC in terms of speed. The simulation results are derived using Cadence environment. The results show that the comparator has 6-bit resolution and power consumption of 4.13 mw for the worst-case frequency of 250 MHz. It fulfills all the performance requirements, most of them with large margins.*

Keywords: ADC