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Design of Hybrid Memory Logic Based Built in self-test for Memory Testing

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Abstract*:* *Microprocessors, microcontrollers, multi-core systems, and multi-processor systems are just a few of the many places where built-in self-test (BIST) modules would be invaluable. Traditional BIST modules cannot remedy the issues in different memories caused by stopped at faults. Errors in memory elements can be detected and fixed with the help of a Hybrid Memory Logic (HML)-BIST, the emphasis of this work. Initial implementations made use of linear feedback shift register (LFSR) modules to generate random test patterns for data writing, address writing, and address reading. Here, non-repetitive random numbers are generated using LFSR using the activity factor. The information in RAM is then compared to the raw data in the original source. The BIST component then fixes the stored data after running the tests. The simulation results showed that the suggested HML-BIST method outperformed the existing methods in terms of area, latency, and power.*

Keywords: BS-LFSR (bits wapped LFSR), LFSR (linear feedback shift register), single stuck-at faults, 8x8 BCD multiplier, Double Dabble algorithm

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