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An Efficient VLSI Design of Pipelined Half Precision Floating Point ALU Design

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Abstract: *The IEEE Standard 754 floating point number is the most popular format for real numbers in modern computers. This work provides an overview of IEEE floating point and its representation is provided in this work. Using half-precision arithmetic in Verilog for VLSI design involves translating data models into half-precision floating-point number and creating the appropriate arithmetic operations. The IEEE 754 standard defines the structure of half-precision floating-point number consisting of 16 bits divided into three parts: a sign bit, a five-bit exponent, and a ten-bit mantissa. The sign bit represents the sign of the number, the exponent represents the magnitude of the number, and the signific and or mantissa represents the precision of the number. To use half-precision arithmetic in Verilog, you must create a module that defines the half-precision floating-point number data structure and uses the arithmetic operators for addition, subtraction, multiplication, and square. This pipeline, described on Verilog, is built on a Xilinx Spartan 3 FPGA. Xilinx Timing Analyzer was used measure the runtime. Also, when compared to cutting-edge technology, our offering outperforms them in terms of latency and throughput. ALU Design is known by Proposed Arithmetic Operation*

Keywords: ALU Design

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